Parallel Operation of Inverters With Isolated DC Link for Minimizing Sharing Inductor

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***Abstract*—In this paper, it is described how the circulating current flows between inverters that have isolated dc link such as cascaded H-bridge (CHB) topology when they are operating in parallel. In this case, zero sequence circulating current, which normally flows through shared dc link, cannot flow between inverters in parallel. However, circulating current is provoked by asynchronous switching instant of devices, difference of dc-link voltages of parallel inverters, and unbalanced impedance. The circulating current should be suppressed by a sharing inductor that is inserted between inverters. Generally, all of the inverters should synthesize the same output voltage reference for load current control to minimize the size of this sharing reactor. However, this conventional method cannot guarantee diminishing circulating current in the transient state and even in the steady state. In this paper, in order to reduce sharing reactance, after deriving circulating current model from general case of n-parallel operation, circulating current control method is devised based on the model. This proposed algorithm is applied to active front end five-level-CHB inverter system for medium voltage drive. Simulation and experimental results are provided to verify the effectiveness of the proposed control scheme.**

***Index Terms*—Active front end (AFE) five-level cascaded H-bridge (CHB), CHB, circulating current, parallel operation, sharing reactorcc.**

I. Introduction

BY PARALLEL operation, multiple inverters which have the same power capacity can be applicable to a motor drive system with higher power capacities. It can make system be designed as modular structure. It may result in reduced production and maintenance cost of overall motor-drive system. Besides, even if one of the inverters fails, the motor still can be driven continuously with reduced power capacity. And, it can enhance system reliability [1]–[8]. Due to these advantages, parallel operation of inverters has been applied to many industrial fields, as well as large medium voltage drives [2], [5], [7].

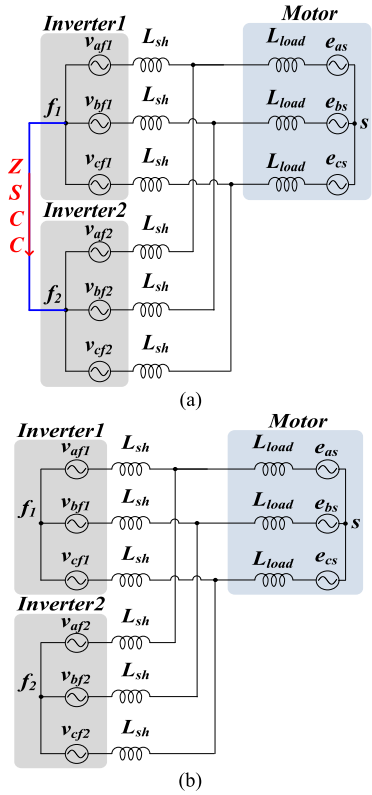

Fig. 1. Type of parallel operation. (a) Non-isolation type. (b) Isolation type.

Fig. 1 briefly shows two types of paralleled inverter system according to whether dc link is isolated or not. Fig. 1(a), where f_1 and f_2, neutral points of inverters are connected, shows inverter with nonisolated dc link. In this case, due to common dc link, a considerable amount of zero sequence circulating current (ZSCC) inevitably flows between inverters connected in parallel [9]–[12], following blue line from f_1 to f_2. Many research works on controlling ZSCC have been carried out. According to these research works, zero vectors are utilized to prevent ZSCC

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[12]–[16]. Fig. 1(b), where f_1 and f_2, neutral points of inverters are not connected, shows inverters with isolated dc link. In this case, ZSCC cannot flow, because there is no path for zero sequence current. However, in this type of paralleled system, the overall system is bulky and costly, because of additional dc power supplies or the ac line frequency transformer with multiple windings [3].

Cascaded H-bridge (CHB) is the most widely used inverter topology for motor drive, because of the benefits including modularity, redundancy, low switching frequency, and low total harmonic distortion (THD) [18]. Each cell in CHB has an isolated dc link because inverters on the grid side in the cell are fed by isolated ac source through multiwinding input transformer. Generally, the inverter for the motor drive is directly connected to a motor without filtering inductor except the inductor for suppression of dv/dt due to switching of insulated gate bipolar transistor (IGBT), because of inherent inductance of its stator winding [4].

However, in parallel operation, sharing inductor should be employed in parallel path, because the inverter is considered as a voltage source, as shown in Fig. 1. Therefore, one of the important issues is to reduce size of the sharing inductor in order to minimize cost and volume/weight of the overall system. For minimizing sharing reactor, paralleled inverters employ synchronized carrier and synthesize the same voltage reference. When it is assumed that each inverter has the same magnitude of dc-link voltage and operates in ideal condition, any current cannot conduct in parallel path. Then, it can be said that it would be the best pulse-width modulation (PWM) scheme under ideal condition. Therefore, this PWM scheme has been usually employed in order to minimize sharing inductor.

It is important to choose an appropriate inductor type as sharing inductor in terms of cost and size reduction. There are several types of inductor. Coupling inductor is generally used with interleaved PWM [5], [7]. However, it is not a proper solution for synchronized PWM. Also, three single phase inductors could be considered as sharing inductor because it can significantly reduce ZSCC by common mode impedance of each inductor. In the case of parallel operation of isolated inverters, which is the system in this paper, there is no path for ZSCC as aforementioned. Therefore, three single phase inductors are not a cost-effective solution for the system under consideration. Instead, an EI core inductor, one of the most widely used core structure, can be employed and provides cost and size benefits. It is possible to minimize its size under the same inductance because summation of fluxes induced by three-phase balanced voltage source is null. As a result, EI core inductor is selected as the sharing inductor in this paper.

In the real system, even if all the inverters in parallel synthesize the same output voltage, their pole voltages would not be the same, because they are affected by modulation conditions such as turn ON/OFF time delays of switching devices, $T_{\rm on}$, $T_{\rm off}$, depending on its temperature, and gate signal propagation delay of each switch of each inverter. Besides, the unbalanced impedance between the phase of the sharing reactor and the inverter itself comes from various reasons such as asymmetric flux linkage from EI core and unequal internal impedance of device. These nonideal conditions could make unbalanced current in parallel

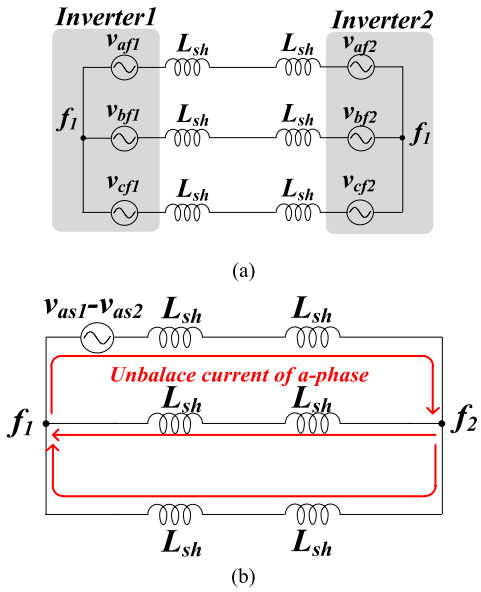

Fig. 2. Circulating current when isolated inverters operating in parallel. (a) Parallel path of 2 parallel operation of non-isolation type. (b) Unbalance current of a-phase.

operation of isolated inverters [4]. Fig. 2 shows the example of unbalanced current. Fig. 2(a) shows the parallel path, when load side current through inductor is considered as a current source under the assumption that $L_{\rm sh}$ is much smaller than $L_{\rm load}$. If v_{af1} is not equal to v_{af2} due to aforementioned reasons, a-phase unbalance current would flow through red line in Fig. 2(b). This unbalanced current circulates through the paralleled inverter instead of flowing toward motor. Therefore, the unbalanced current can be considered as a circulating current in a broad sense. Furthermore, this circulating current has an effect on isolated dc-link voltage. Unless the current is damped out by resistance component on parallel path, dc-link voltage difference would be getting larger. This positive feedback would make the system be stalled by over current fault because of current sharing problem between the inverters. Therefore, the circulating current due to the unbalanced current should be controlled appropriately, in order not only to share current properly but also to minimize the reactance of the sharing inductor.

Recently, several medium voltage motor-drive applications such as downhill conveyors demand regeneration capability on the inverter [19]–[22]. In these applications, there were attempts to replace three-phase diode front end (DFE) with three-phase active front end (AFE) [19]. To reduce the complexity and cost of the system, single phase five-level back-to-back converter was employed instead of conventional three-level H-bridge cell with three-phase DFE. [21], [22]. This approach would reduce the number of secondary winding of the input multiwinding transformer by one-third and that of legs per power cell from 5 to 4, compared with three-phase AFE. Therefore, five-level H-bridge cell would cut down the size and cost of the system [21]. Developed control scheme is applied to parallel operation of this topology, as representative inverter with isolated dc link.

In this paper, in Section II, after analyzing the circulating current, the minimum reactance of sharing reactor is determined to limit the peak value of high-frequency component of circulating

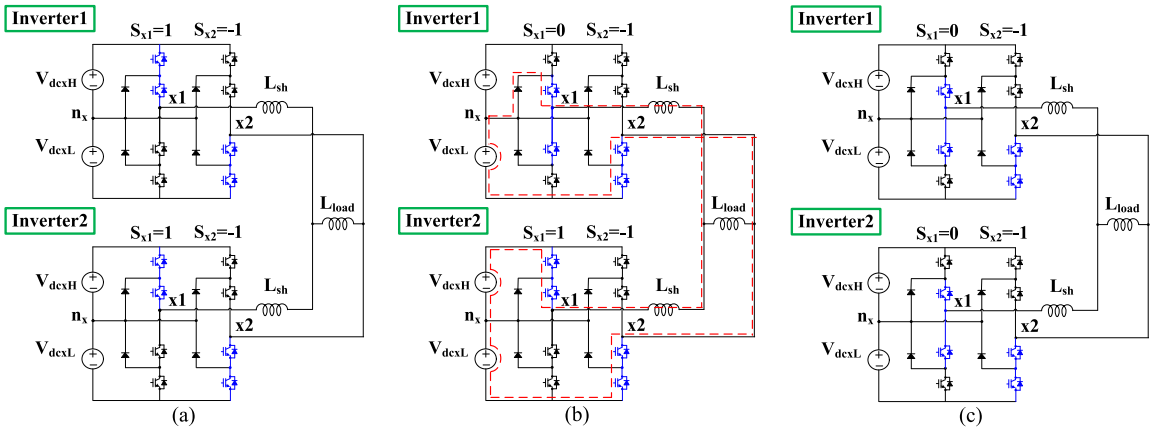

Fig. 3. Example of circulating current provoked by changing switching state asynchronously. (a) Synchronous switching state (start state). (b) Asynchronous switching state. (c) Synchronous switching state (final state).

current. In Section III, an equivalent circuit of circulating current is derived from the general case that arbitrary number of inverters is connected in parallel. Based on the equivalent circuit for circulating current, circulating current controller is devised. Because the circulating current model is derived from a general case of n-parallel operation of inverters by using circuit theory, the developed circulating current controller based on the model is independent of the topology of the inverter. And the design and control methodology can be extended to different types of inverters in parallel with isolated dc link. By using the proposed control scheme, low-frequency components from asynchronous switching of devices, dc-link voltage difference, and unbalanced impedance from sharing inductor, and so on are suppressed simultaneously by using small control voltage. In Sections IV and V, feasibility and validity of the devised method are confirmed by simulation and experimental results. In addition to the previous version of this research [23], a matrix form of the proposed method is included and its stability is analyzed in this paper.

II. Circulating Current

Because parallel operation of isolated inverters is three-phase balanced system, per phase equivalent circuit can be used for the analysis. Fig. 3 describes that a sequence of switching state changes in x-phase of inverters when two 5L-CHB inverters operate in parallel on the load side, where "x" denotes an arbitrary phase among a, b, and c. S_{x1} and S_{x2} represent switching function of leg1 and leg2 in x-phase, respectively. The switching function has three switching states. Three switching states are defined as follows, "1" states that pole voltage of its leg is V_{dcxH}, "0" states that pole voltage of its leg is 0, "–1" states that pole voltage of its leg is $-V_{\mathrm{dcxL}}$. Fig. 3 shows that S_{x1} changes from 1 to 0. Fig. 3(a) and (c) shows the switching state of the parallel inverters at the start and the final, respectively, under the assumption that there is slight time delay in switching of inverter 2 compared with that of inverter1 . In Fig. 3(b), where each S_{x1} of inverters in parallel has different state, S_{x1} of inverter 1 changes from 1 to 0, before that of inverter 2 changes. This asynchronous switching state due to the different time delay of the gating signal and associated switching of the power semiconductor provokes circulating current like red dashed line in Fig. 3(b) which shows conducting path of the circulating current.

Output voltage of x-phase in inverter is represented as $V_{\mathrm{dc}}/2 \times (S_{x1} - S_{x2})$, where V_{dc} denotes total dc-link voltage. Difference between output voltages of inverter 1 and inverter 2 varies like $0 \rightarrow V_{\mathrm{dcxH}} \rightarrow 0$, when switching state is changed as shown in Fig. 3. It is worthy to note that the voltage source provoking the circulating current can be represented as voltage source with a pulse shape. From this intuition, the maximum of circulating current can be derived. Fig. 4(a) shows the equivalent circuit including the pulse voltage generated by the time delay, Pulse_x, and circulating current, i_{x_cir}, generated by the pulse voltage. In order to analyze the relationship between the pulse voltage and the circulating current, if the current through the load side inductor, L_{load}, is considered as a current source, Fig. 4(a) can be redrawn like Fig. 4(b). By replacing voltage sources as a short circuit and current sources as an open circuit, Fig. 4(b) is simplified to Fig. 4(c). In this system, the maximum pulse voltage is V_{dc}. From this simplified equivalent circuit, peak value of circulating current, $i_{x\_\mathrm{cir}}|_{\mathrm{peak}}$, can be represented as (1), where T_{delay} is the maximum difference of switching time coming from a difference of T_{on} and T_{off} of switching device and propagation delay of gating signal.

$$i_{x\_\mathrm{cir}}|_{\mathrm{peak}} = \frac{2V_{\mathrm{dc}}}{3L_{\mathrm{sh}}} T_{\mathrm{delay}}. \tag{1}$$

Equation (1) comes from Fig. 4(c), where dc-link capacitors are considered as an ideal voltage sources with the same value in paralleled inverters. Under the assumption, if $i_{x\_\mathrm{cir}}|_{\mathrm{peak}}$ is determined by hardware and designer requirement, the inductance of sharing inductor, L_{sh}, can be calculated by using (1). However, in the real system, dc-link voltages of each inverter in parallel are neither the same value nor ideal voltage sources. Because of this, circulating current could be larger than the value calculated by (1).

III. Circulating Current Model and Control Method

In this section, so as to suppress the circulating current, a circulating current model is derived from n-paralleled inverters. Due to three-phase balanced circuit, n-paralleled inverters can be

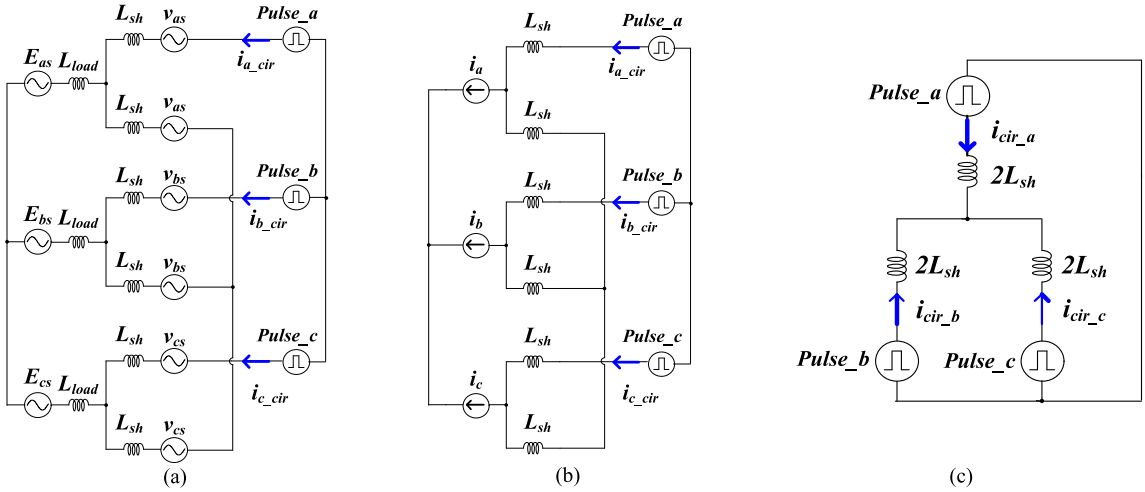

Fig. 4. Equivalent circuit of circulating current. (a) Equivalent circuit including the pulse voltage. (b) Simplified equivalent circuit. (c) Circulating current and pulse voltage model.

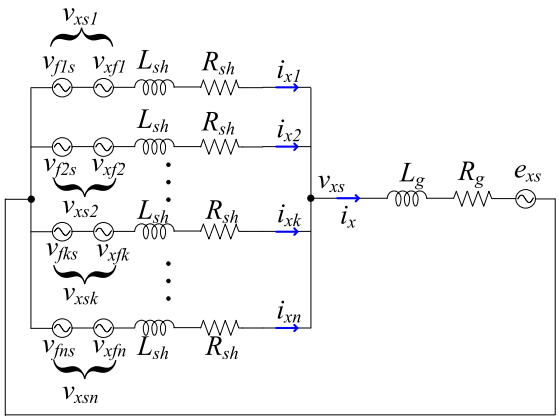

Fig. 5. *x*-phase model in n-paralleled inverters.

simplified to single-phase equivalent circuit through per phase analysis as shown in Fig. 5. Based on this model, a circulating current controller can be devised.

$$
\begin{aligned}
(v_{xs1} - e_{xs}) &= z_{\rm sh} i_{x1} + z_{\rm load} \left(\sum_{k=1}^{n} i_{xk} \right) \\
(v_{xs2} - e_{xs}) &= z_{\rm sh} i_{x2} + z_{\rm load} \left(\sum_{k=1}^{n} i_{xk} \right) \\
&\vdots \\
(v_{xsk} - e_{xs}) &= z_{\rm sh} i_{xk} + z_{\rm load} \left(\sum_{k=1}^{n} i_{xk} \right) \\
&\vdots \\
(v_{xsn} - e_{xs}) &= z_{\rm sh} i_{xn} + z_{\rm load} \left(\sum_{k=1}^{n} i_{xk} \right) \\
\text{where, } Z_{\rm sh} &= R_{\rm sh} + sL_{\rm sh}, \\
Z_{\rm load} &= R_{\rm load} + sL_{\rm load} \qquad (2) \\
i_{xk} &= i_{x\_{\rm av}} + i_{x\_{\rm cirk}} \qquad (3)
\end{aligned}
$$

$$
i_{x\_{\rm av}} = \frac{i_x}{n} = \frac{\sum_{k=1}^{n} i_{xk}}{n} \qquad (4)
$$

$$
\sum_{k=1}^{n} i_{x\_{\rm cirk}} = 0 \qquad (5)
$$

$$
\Sigma(v_{xsk} - e_{xs}) = \Sigma(z_{\rm sh} + nz_{\rm load}) \times i_{x\_av}. \qquad (6)
$$

$$
\frac{\Sigma v_{xsk}}{n} = v_{xs}. \qquad (7)
$$

$$
i_{x\_av} = \frac{\frac{\Sigma v_{xsk}}{n} - e}{(z_{\rm sh} + nz_{\rm load})} = \frac{v_{xs} - e}{(z_{\rm sh} + nz_{\rm load})}. \qquad (8)
$$

By applying Kirchhoff's voltage law (KVL) to n branches connected in parallel like Fig. 5, n equations are given as (2). Current conducting through the kth branch of x-phase, i_{xk}, is defined as the sum of an average current, $i_{x\_{\rm av}}$, and a circulating current, $i_{x\_{\rm cirk}}$, like (3), where an average current is defined as (4). Sum of circulating currents becomes null from that of all of branch currents, as shown in (5). Sum of KVL equations, (2), can be rewritten as (6). Equation (7) is given by the fact that summation of voltage of sharing inductor from circulating current also becomes null because of (5). By using (7), the average current model could be simplified like (8).

Output phase voltage of the kth branch, v_{xsk}, is defined as the sum of v_{xs} and difference voltage, Δv_{xs}, like (9). Equation (10) is given by substituting (9) into v_{xsk} in (2). This equation means that the difference voltage is a degree of freedom to control the circulating current directly. Therefore, v_{xsk} consists of two voltage components. One is the output voltage, v_{xs}, in order to control the average current. The other is the difference voltage, Δv_{xs}, for controlling the circulating current. Equation (11) is deduced by summing KVL equations, (2). Based on these equations, (8) and (10), the average current and the circulating current, both, would be controlled independently.

The circulating current model in (12) is derived without any assumption, as aforementioned. It is ideally decoupled from the output current i_x. However, voltage limitation of each inverter under given dc-link voltage is not considered. It is the only case

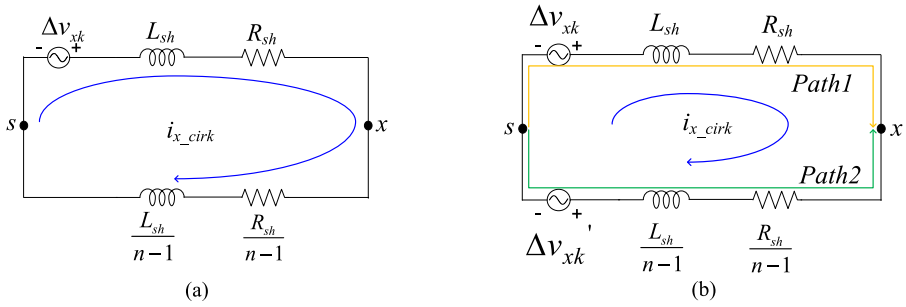

Fig. 6. x-phase model simplified equivalent model in case of n-paralleled inverters. (a) x-phase, kth branch unbalance circulating current model. (b) x-phase, kth branch unbalance circulating current model with compensating voltage, $\Delta v_{xk}{}'$.

that the circulating current and the output current are coupled. For example, after voltage to control circulating current is added to v_{xs}, the voltage, v_{xsk}, can be clamped by voltage limitation of the kth inverter because of its dc-link voltage. It makes the output current be distorted. If only the voltage source of the kth branch to suppress the circulating current of the kth branch is considered, then the x-phase model in Fig. 5 can be simplified to Fig. 6(a). According to Fig. 6(a), difference between potential of two nodes, x and s, is induced by voltage dividing of Δv_{xk}. In other words, this voltage source, Δv_{xk}, can affect the output voltage v_{xs}. To eliminate this influence on the output voltage, both additional voltage source Δv_{xk} and another compensating voltage source $\Delta v'_{xk}$ could be added to the equivalent circuit, as shown in Fig. 6(b). In Fig. 6(b), wherepath1 and path2 are defined, voltage sum of path 1 and path 2 would be null by KVL, if the additional voltages are defined as (12). As a result, if all of the branches are considered by applying the superposition principle, total compensation voltage, $\Delta v_{xk\_\mathrm{comp}}$ is defined as (13). It is converted to matrix formation in (14) as follows:

$$v_{xsk} = v_{xs} + \Delta v_{xk}. \tag{9}$$

$$\Delta v_{xk} = z_{\mathrm{sh}} i_{x\_\mathrm{cirk}} \tag{10}$$

$$\Sigma \Delta v_{xk} = 0 \tag{11}$$

$$\Delta v_{xk} = z_{\mathrm{sh}} i_{x\_\mathrm{cirk}} \tag{12}$$

$$\Delta v_{xk}{}' = -\frac{z_{\mathrm{sh}}}{n-1} i_{x\_\mathrm{cirk}} = -\frac{\Delta v_{xk}}{n-1}$$

$$\Delta v_{xk\_\mathrm{comp}} = \Delta v_{xk} - \frac{1}{n-1}\sum_{i\neq k}^{n} \Delta v_{xi}. \tag{13}$$

Based on the circulating current suppression model and method, equivalent control loop including the circulating current model and the proposed controller can be depicted as shown in Fig. 7, where I_{abc_cir} is defined by (15). I_{abc_cir} is converted to d-, q-axis current on the synchronous reference frame, $I^{e}_{dq\_\mathrm{cir}}$, by using rotating vector, $R(\Theta_r)$. Their reference, $I^{e*}_{dq\_\mathrm{cir}}$, is generally set as null. Based on this figure, closed-loop function, $i^{e}_{dq\_\mathrm{cirk}}/i^{e*}_{dq\_\mathrm{cirk}}$ can be written as (17) if cross-coupling term due to rotation of the reference frame $j\omega_r L_{\mathrm{sh}} i^{e}_{dq\_\mathrm{cirk}}$, is decoupled by feed forwarding term. Circulating current gains of circulating current controller, k_{psh} and k_{ish} can be set as (17), in order to make the transfer function of this closed-loop function be first-order low-pass filter (LPF) with bandwidth, ω_{sh}.

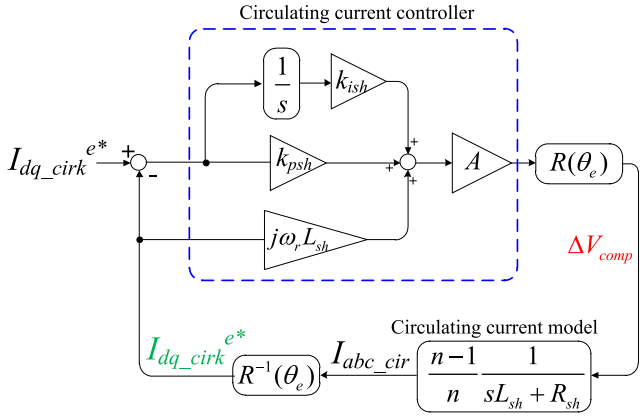

Fig. 7. Circulating current model and proposed circulating current controller.

ΔV_{comp} is defined as (16), and added to each phase voltage reference, v_{xs} like (9) instead of Δv_{xk}.

According to (17), because the closed-loop function is a first-order LPF, this system is stable regardless of ω_{sh} under the ideal condition. However, in the real system, there are digital signal processing delay and PWM delay. Because of these delays, system would be unstable when ω_{sh} is too large even if parameters of the plant are exactly known. Therefore, in order to find out stable condition according to ω_{sh}, stability of the closed control system should be analyzed in the z-domain.

$$\Delta v_{x\_\mathrm{comp}} = A \cdot \Delta v_x$$

where,

$$\Delta v_{x\_\mathrm{comp}} = \begin{bmatrix} \Delta v_{x1\_\mathrm{comp}} \\ \Delta v_{x2\_\mathrm{comp}} \\ \vdots \\ \Delta v_{xk\_\mathrm{comp}} \\ \vdots \\ \Delta v_{x(n-1)\_\mathrm{comp}} \\ \Delta v_{xn\_\mathrm{comp}} \end{bmatrix}, \Delta v_x = \begin{bmatrix} \Delta v_{x1} \\ \Delta v_{x2} \\ \vdots \\ \Delta v_{xk} \\ \vdots \\ \Delta v_{x(n-1)} \\ 0 \end{bmatrix}, A = \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_k \\ \vdots \\ \alpha_{n-1} \\ \alpha_n \end{bmatrix}$$

$$\alpha_k = \begin{bmatrix} \beta_1 & \beta_2 & \cdots & \beta_k & \cdots & \beta_{n-1} & \beta_n \end{bmatrix}$$

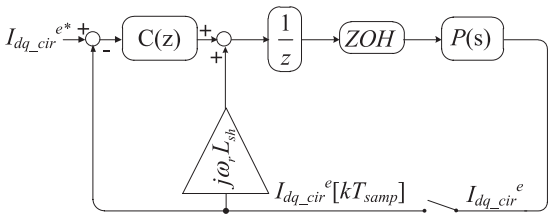

Fig. 8. Complex vector block diagram of the proposed synchronous current controller.

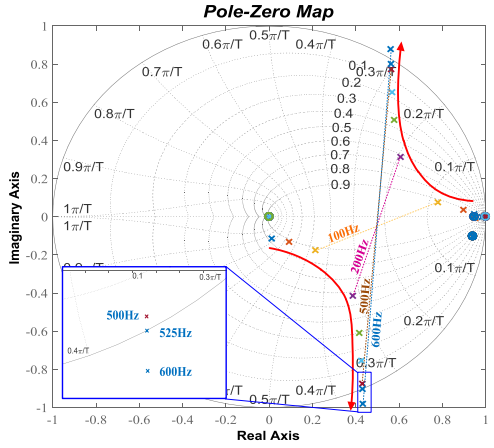

Fig. 9. Complex vector root locus of closed loop with the proposed controller according to its control bandwidth in the z-domain.

$$\beta_m = \begin{cases} m = k: & \beta_m = 1 \\ m \neq k: & \beta_m = -\dfrac{1}{n-1} \end{cases}. \tag{14}$$

$$I_{abc\_cir} = \begin{bmatrix} I_{a\_cir} & I_{b\_cir} & I_{c\_cir} \end{bmatrix}$$

where, (15)

$$I_{x\_cir} = \begin{bmatrix} i_{x\_cir1} & \dots & i_{x\_cirn} \end{bmatrix}.$$

$$\Delta V_{comp} = \begin{bmatrix} \Delta v_{a\_comp} & \Delta v_{b\_comp} & \Delta v_{c\_comp} \end{bmatrix} \tag{16}$$

$$\frac{i_{dq\_cirk}^{e}}{i_{dq\_cirk}^{e*}} = \frac{\dfrac{sk_{psh} + k_{ish}}{s}}{1 + \dfrac{sk_{psh} + k_{ish}}{s}\dfrac{1}{sL_{sh} + R_{sh}}} = \frac{\omega_{sh}}{s + \omega_{sh}}$$

where,

$$k_{psh} = \omega_{sh} L_{sh},\ k_{ish} = \omega_{sh} R_{sh}. \tag{17}$$

Fig. 8, where $P(s)$ is a plant and $C(z)$ is a digital PI-controller, shows complex block diagram including digital delays. Equation (18) shows the circulating current model on the synchronous reference frame. The integrator in $C(z)$ using Euler's backward formula yields (19). PWM delay and digital delay are considered as zero-order hold, ZOH and unit delay z^{-1}. $P(z)$ in (20) is a result of discretization of $P(s)$. Equation (21) is a closed-loop function from d-, q-axis circulating current reference to d-, q-axis circulating current on the synchronous reference frame. By using the equation, according to the variation of the bandwidth ω_{sh}, system stability can be analyzed in z-domain. Fig. 9 shows loci of poles when bandwidth, ω_{sh} is getting larger from 62.8 rad/s, 10 Hz to 3770 rad/s, 600 Hz, when simulation parameters in Table I is used. According to this pole zero map, when ω_{sh} is over 628 rad/s, 100 Hz, damping is steeply decreased. Besides, when ω_{sh} is over about 3267 rad/s, 520 Hz, the system would be unstable. Therefore, based on this result, ω_{sh} is set as 628 rad/s, 100 Hz in the case of simulation. Also, the bandwidth in case of experiment can be determined by the same manner.

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Rated power	0.417 MW, 4 parallel
Rated voltage (line to line)	2.2 kV_{llrms}, 60 Hz
Rated current	109 Arms, 4 parallel
R_{load}	0.07 Ω [0.024 p.u.]
L_{load}	1.5 mH [0.194 p.u.]
L_{sh}	60 μH [0.002 p.u.]
R_{sh}	11.6 mΩ [0.001p.u.]
T_{delay} (Inv1, Inv2)	400 ns
T_{delay} (Inv1, Inv3)	800 ns
T_{delay} (Inv1, Inv4)	800 ns
C_{dc}	1800 μF

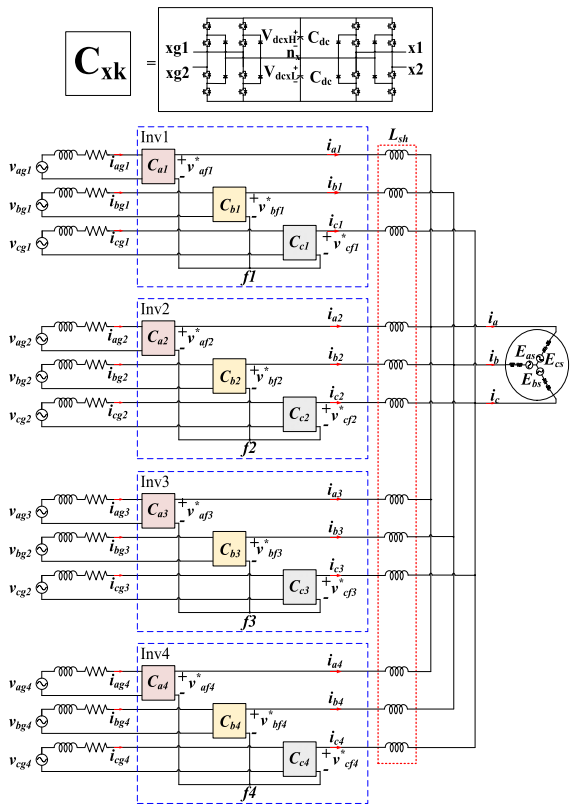

Fig. 10. Simulation model: Four parallel AFE 5L-CHB.

$$P(s) = \frac{1}{sL_{sh} + R_{sh} + j\omega_r L_{sh}} \tag{18}$$

$$C(z) = k_{psh} + k_{ish}\frac{z}{z-1}T_{samp} \tag{19}$$

$$P(z) = Z\{\mathrm{ZOH} \cdot P(s)\} = (1 - z^{-1})Z\left\{L^{-1}\left\{\frac{1}{(s + j\omega_r)L_{sh} + R_{sh}}\frac{1}{s}\right\}\right\} \tag{20}$$

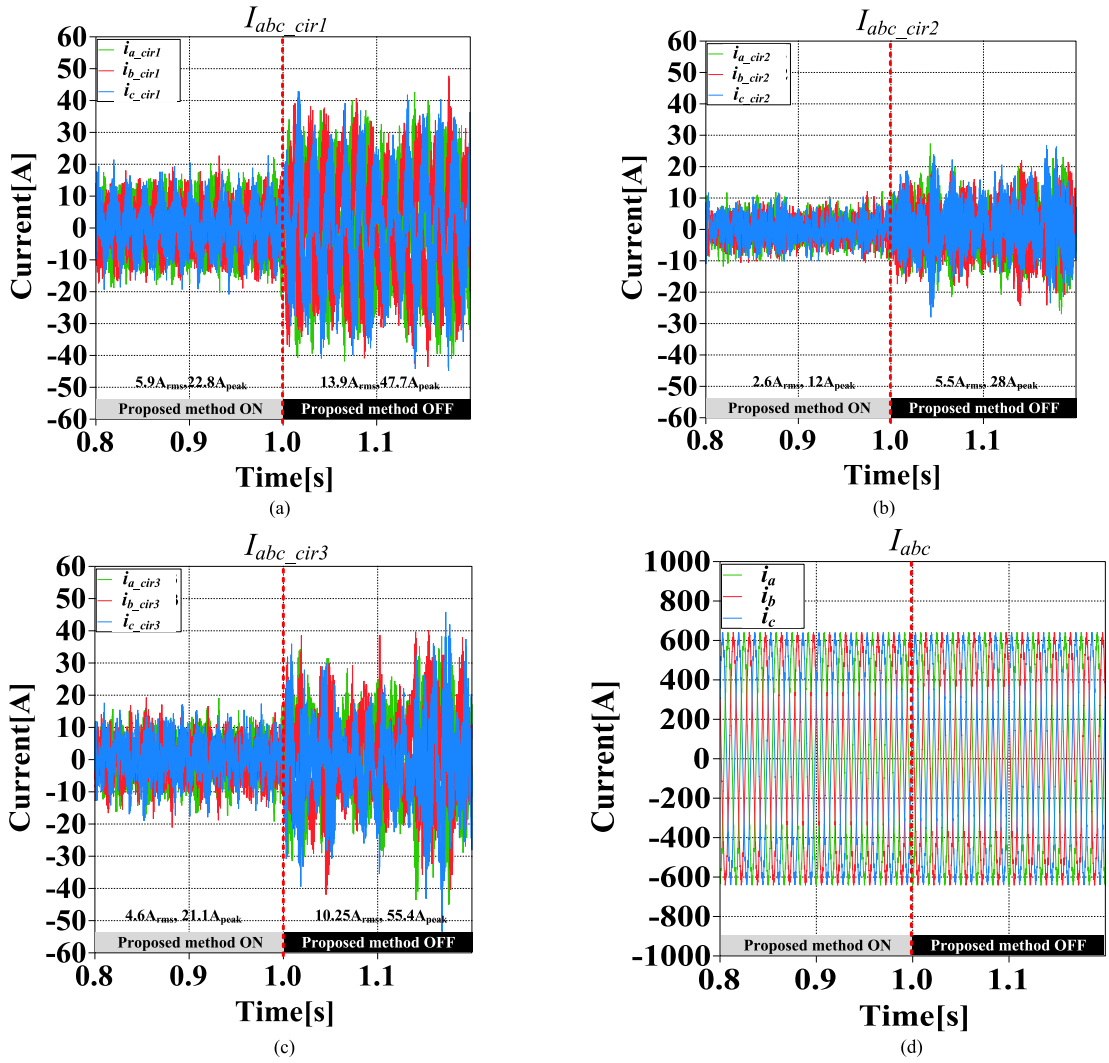

Fig. 11. Simulation results: (a) I_{abc_cir1}; (b) I_{abc_cir2}; (c) I_{abc_cir3}; and (d) total current, I_{abc}.

TABLE II
EXPERMENTAL PARAMETER

Parameter	Value
Rated power	11 kW
Rated speed	377 rad/s
Pole number	4
Rated torque	58 N·m
Sharing inductor($L_{\rm sh}$)	80 μH [0.01 p.u.]

$$\frac{i_{dq}^{e}}{i_{dq}^{e*}} = \frac{C(z) \times z^{-1} \times P(z)}{1 + C(z) \times z^{-1} \times P(z) - j\omega_g L_g \times z^{-1} \times P(z)}. \tag{21}$$

IV. SIMULATION RESULT

Simulation is conducted with MATLAB to verify the circulating current model and the effectiveness of the proposed control method. In the simulation, four parallel AFE 5L-CHB inverters are employed for current control in R–L load with 1720 V, 60 Hz, ideal voltage source. These parameters are deduced from 1.67 MW induction machine (IM) drive system and listed in Table I. Each x-phase compensation voltage is written by (22), according to (14).

Simulation configuration is shown in Fig. 10. To show the validity and effectiveness of the proposed suppression method, the proposed circulating current controller is engaged from 0.5 to 1 s and disengaged after 1 s.

In Fig. 11, simulation results are shown. When the proposed method is engaged, the circulating currents of Inv 1, Inv 2, Inv 3, and Inv 4 ,are well regulated under 5.9 $A_{\rm rms}$, 22.8 $A_{\rm peak}$. Those values in per-unit are 0.05 and 0.15 p.u., respectively. However, after disengagement of the controller at 1 s, root mean square (RMS) and maximum of circulating current increase by about 200% or 260% of the current before disengagement of the controller.

$$\Delta v_{x1\_\rm comp} = \Delta v_{x1} - \Delta v_{x2}/3 - \Delta v_{x3}/3$$

$$\Delta v_{x2\_\rm comp} = \Delta v_{x2} - \Delta v_{x1}/3 - \Delta v_{x3}/3$$

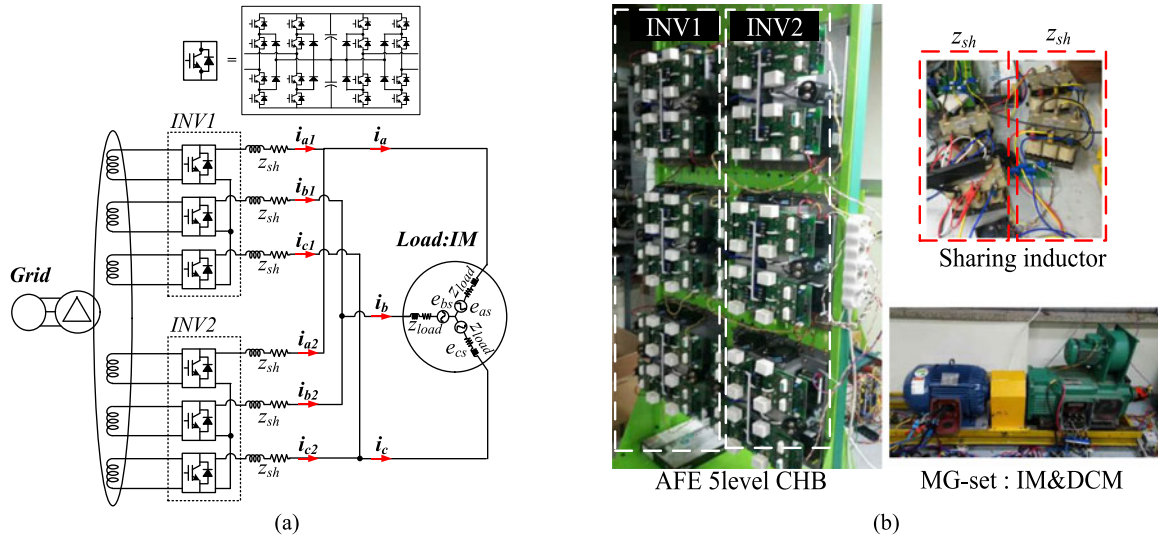

Fig. 12. Experimental circuit and set-up under test. (a) Circuit under experimental test. (b) Experimental set-up.

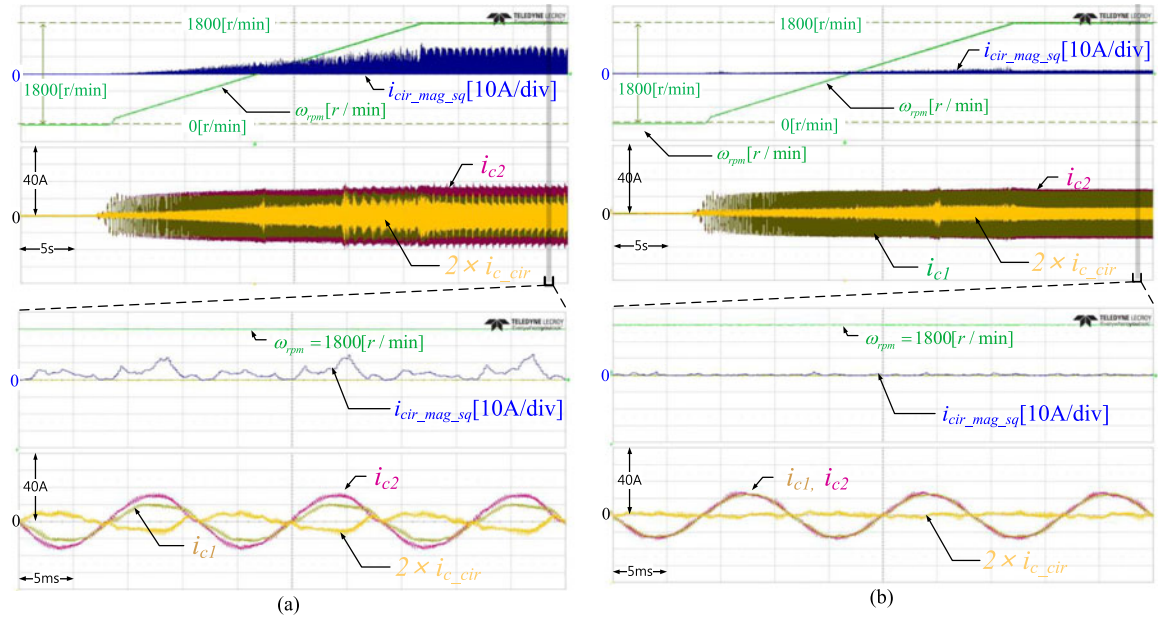

Fig. 13. Experimental results: Acceleration mode under no load condition. (a) Without circulating current suppression control. (b) With circulating current suppression control.

$$\Delta v_{x3\_\mathrm{comp}} = \Delta v_{x3} - \Delta v_{x1}/3 - \Delta v_{x2}/3$$
$$\Delta v_{x4\_\mathrm{comp}} = -\Delta v_{x1}/3 - \Delta v_{x2}/3 - \Delta v_{x3}/3. \quad (22)$$

V. Experimental Result

Fig. 12 shows the experimental setup for verifying the proposed scheme which suppresses the circulating current. Two paralleled inverter system ($n = 2$) with AFE 5L-CHB is shown in Fig. 12(a). This configuration has been implemented as shown in Fig. 12(b). The parameters of IM and sharing inductor are listed in Table II. The IM is driven by V/F control and a dc motor is used as a load machine. The dc-link voltage reference of each cell and switching frequency are 350 V and 2.5 kHz, respectively. Compensation voltage for circulating current is derived as $\Delta v_{x1\_\mathrm{comp}} = \Delta v_{x1}$ and $\Delta v_{x2\_\mathrm{comp}} = -\Delta v_{x1}$ from (14).

Square of circulating current magnitude, $i_{\mathrm{cir\_mag\_sq}}$, is defined as (23), by using stationary d-, q-axis currents, i_{ds_cir}, i_{qs_cir}. This variable can be used as an index of how much circulating current is reduced by the proposed method because it represents the amount of total circulating current. Besides by using this value, RMS value of circulating current can be easily calculated by

$$i_{\mathrm{cir\_mag\_sq}} = {i_{ds\_\mathrm{cir}}}^2 + {i_{qs\_\mathrm{cir}}}^2 \quad (23)$$
$$\mathrm{RMS} = \sqrt{\mathrm{average}(i_{\mathrm{cir\_mag\_sq}})}. \quad (24)$$

Fig. 13 shows experimental results, when the IM is accelerated from standstill to the rated speed, under no load

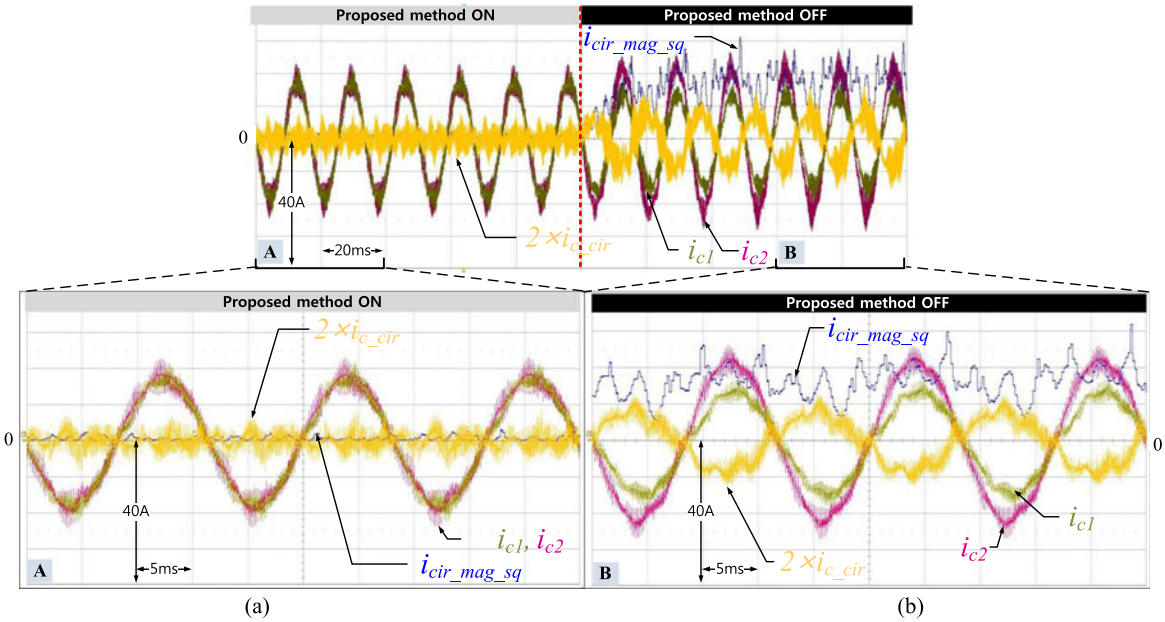

Fig. 14. Experimental results 2: steady state under 75% load condition at rated speed. (a) Expanded waveform with proposed method. (b) Expanded waveform without proposed method.

condition. In Fig. 13(a), where the circulating currents are not controlled, the maximum circulating current is 3.9 A_{peak}, that is, 0.19 p.u. and its RMS value calculated by (24) is 2 $A_{\rm rms}$, that is, 0.14 p.u. Fig. 13(b), where the proposed circulating current control method is engaged, the maximum peak circulating current and its RMS value are cut down to 8.8%, 33.7% compared to the value before engagement of the controller, respectively.

Fig. 14 shows steady-state waveform under 75% load condition at the rated speed. When the proposed method is engaged, the RMS value of the circulating current is 0.72 A_{rms} which is 0.05 p.u. and the maximum circulating current is 1.48$A_{\rm peak}$ which is 0.07 p.u. After the proposed scheme is disengaged, the RMS value of the circulating current reaches 3.4 $A_{\rm rms}$(0.24 p.u.) and maximum circulating current is 5.7 $A_{\rm peak}$(0.28 p.u.). In other words, by employing the proposed method, RMS and maximum of the circulating current are decreased to 21.2% and 26% of the value before engagement of the controller, respectively.

It is demonstrated from above experimental results that under overall operating condition, the drive system can work well with much less circulating current through the proposed suppression method. The magnitude of voltage to control the circulating current is only below 3 V, which is only 0.86% of the rated voltage of dc link. Also, the peak values of circulating currents are suppressed below 2 A, which is 3.6% of the rated load current, at any load. However, without the proposed control, the drive system fails under the same load condition, due to over current protection that limits the maximum current level of the system.

VI. Conclusion

In this paper, the phenomenon regarding the circulating current coming from the imbalance between paralleled inverters, which have isolated dc link such as CHB topology, has been analyzed. A general equivalent circuit model to calculate the circulating current has been deduced from n-paralleled inverter case. Based on this model, a scheme to suppress the circulating current has been proposed and implemented. Also, a guideline of the gain setting of the controller has been presented. Finally, the validity, feasibility, and effectiveness of the proposed method have been verified by simulation and experimental results. By using the proposed method, the circulating current of the drive system has been suppressed effectively and also the drive system can be free from overcurrent fault due to the circulating current.

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