DC-Link Voltage Stabilization for Reduced DC-Link Capacitor Inverter

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***Abstract*—In conventional motor drive systems using pulsewidth modulation (PWM) inverters, large electrolytic capacitors are used for stabilization of the dc-link voltage. Since the electrolytic capacitors are bulky and reduce reliability of the system due to short lifetime, there have been many efforts to eliminate or reduce the electrolytic capacitors in the motor drive system. However, the PWM inverter with reduced dc-link capacitor has a problem that the dc-link voltage is less stable compared to the conventional inverter because the capability of storing energy is also reduced. In this paper, a dc-link voltage stabilization algorithm using an active damping is proposed so that the dc-link voltage can be stabilized with reduced dc-link capacitor. To achieve load-/source-independent stabilization, a source state estimator which estimates both source voltage and current is also proposed. The fluctuation of the dc-link voltage due to a step load change can be also suppressed under the tolerance range using the estimated source current. The effectiveness of the proposed methods is evaluated by experimental results.**

***Index Terms*—Active damping, constant power load (CPL), dc-link capacitor, dc-link voltage stabilization, electrolytic capacitor, pulsewidth modulation (PWM) inverters.**

I. Introduction

THE DC-LINK capacitors in the pulsewidth modulation (PWM) inverter act as an energy buffer to stabilize the dc-link voltage and to keep it almost constant. Thus, electrolytic capacitors with large capacitance per unit volume have been commonly used as the dc-link capacitors. However, the electrolytic capacitors in the dc-link are bulky and make the inverter less reliable because of their short lifetime expectancy. Moreover, the large dc-link capacitance causes the larger total harmonic distortion of the input source current when a three-phase passive rectifier such as a three-phase diode rectifier is used as a front-end. As a result, there have been efforts to replace the electrolytic capacitors with a small film capacitor [1]–[9].

However, the dc-link voltage of the inverter with reduced dc-link capacitance may be unstable, resulting in overvoltage or undervoltage faults if the source inductance is large compared to the dc-link capacitance. This issue becomes significantly serious in the case that the inverter is supplying power to constant power loads (CPLs). It is well known from literature that the CPL may lead the instability of the system due to its so-called "negative impedance" characteristic [10]–[24]. When the dc-link voltage is increasing, the load current is getting smaller so as to maintain constant power to the load. This interaction between the dc-link side and the load side can result in overvoltage or undervoltage at the dc-link.

The aforementioned instability problem can be solved by designing the input filter whose parameters satisfy the stability criterion presented in [10], [13], and [23]. In [10] and [13], the instability due to the CPLs was analyzed using linearization of the CPLs, whereas the input admittance has been analytically expressed in [23] for prediction of dc-link instabilities. However, the required filter inductance to smoothen the source current may be larger than the value that meets the stability criterion. If the parameters of the input filter cannot meet the criterion for this reason, adding some damping resistors at the filter inductors can be an alternative solution to increase the effective damping of the system. In [24], various passive damping circuits, which are added to the filter elements, are presented. However, the damping resistors increase cost and physical size of the system. Thus, there have been many researches to deal with this problem without adding the damping resistors not only in the motor drive applications but also in the dc–dc converter applications [20]–[22].

In [10]–[19], the fluctuating dc-link voltage is actively stabilized by changing the dynamic impedance seen from the dc-link to be positive. Changing impedance of the load can be achieved by modifying the torque-producing current commands of the motor because the output power is directly related to the torque [10]–[15]. However, if the frequency of the dc-link voltage fluctuation is beyond the current control bandwidth, it is not easy to change the dynamic impedance correctly because there may be a relatively large time lag between the motor current commands and the real motor currents.

To overcome this problem, voltage commands, instead of current commands, can be directly perturbed in the case that the frequency of the dc-link voltage fluctuation is beyond the current control bandwidth. The voltage perturbation techniques have been widely used for V/f-controlled permanent-magnet motor drives. Since the permanent-magnet motors without damper windings do not assure the synchronization of the motor under open-loop V/f control, it may be expected to exhibit instability of the rotor motion. In [26] and [27], the stability of the drive was improved by incorporating a stabilizing control

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which utilizes dc-link current feedback or motor current feedback. Similarly, the instability problems due to the reduce dc-link capacitor can be mitigated by modifying the output voltage commands [16]–[18]. In [16], it is assumed that the input source voltage is a constant dc in order to employ a linearized control law. However, due to this assumption, the effectiveness of the active damping is assured only where the source voltage is invariant because the changed impedance is directly related to the dc-link voltage. In the damping method in [18], the dc-link capacitor current is measured and used in making a damping signal, which is injected to the voltage reference. Due to the low-pass filter used to attenuate high-frequency components in the dc-link voltage, it is not hard to suppress high frequency resonance in the dc-link voltage. In [17], the high-pass-filtered dc-link voltage signal is used in making the damping voltages; however, the influence of the high-pass filter was not analyzed sufficiently. The high-pass or bandpass filter, which is typically employed to get the resonance component of the dc-link voltage in [10]–[18], cannot completely attenuate the source voltage fluctuation resulting from the rectification of the three-phase grid especially if the resonance frequency is close to the sixth harmonic frequency of the grid. Thus, it is hard for those stabilization controllers to selectively suppress the resonance.

In addition to the aforementioned issue, the rapid load changes can also result in the dc-link overvoltage or undervoltage [25]. If the diode-rectifier front-end is used in the motor drive, the system cannot manage the regenerative energy from the motor. Hence, the regenerating operation of the motor should be prohibited. In order to prevent the motor from generating power back to the dc-link, the motor torque reference is always kept positive or equal to zero. Even though the regenerated energy from the mechanical power can be blocked by limiting the motor torque reference, the energy stored in both the motor inductance and the filter inductance can be dumped into the dc-link capacitor, resulting in overvoltage at the dc-link. For instance, there will be a voltage spike at the dc-link when the output power decreases stepwise since the energy stored in both inductances moves to the dc-link rapidly. On the other hand, if the output power increases rapidly, there will be a voltage dip at the dc-link since the energy stored in the capacitor is not enough to maintain the dc-link voltage. This phenomenon is because the capability of storing energy of the dc-link capacitor is so weak that the energy stored in the filter inductance and the motor inductance cannot be managed. The simplest approach to prevent this transient dc-link voltage fluctuation is slowing down the response of the inverter (or reducing the control bandwidth). In that case, however, it is inevitable that overall performance would be degraded because of the reduced control bandwidth.

In this paper, a novel dc-link voltage stabilizing method is proposed. The stabilization is basically based on the active damping which actively changes the dynamic impedance of the system by directly modifying the inverter output voltage. In order to make the stabilization not affected by the source voltage variation, the estimated source voltage and the dc-link voltage are utilized in the proposed control law. To estimate the source states (source voltage and source current), a closed-loop estimator to predict the source states is also proposed.

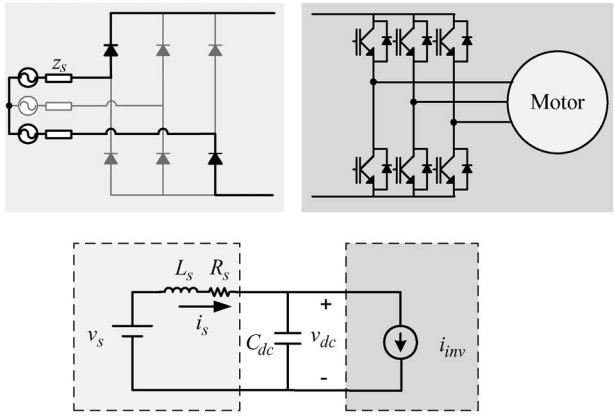

Fig. 1. Simplified model of the motor drive system employing a PWM inverter.

Furthermore, a simple dc-link voltage regulation method to suppress the transient dc-link voltage fluctuation due to the rapid load change is also proposed. In the proposed method, the inverter output voltage is directly modified using both the predicted dc-link voltage and the source current from the estimator. Using the proposed methods, the dc-link voltage can be kept stable without any fault from both the instability due to the CPL and the dc-link voltage fluctuation due to the rapid load change.

This paper is organized in the following manner. Section II presents a model of the conventional motor drive system and describes the instability problem due to the CPL. In Section III, the algorithms used to stabilize the dc-link voltage are proposed. Experimental results are presented in Section IV to verify the proposed algorithms.

II. Instability due to Reduced DC-Link Capacitor

A simplified model of the motor drive system employing a PWM inverter is shown in Fig. 1. The input side source can be modeled as a voltage source and an equivalent series impedance even though the power source is composed of a three-phase diode rectifier and a three-phase grid, because only two of the six diodes of the rectifier conduct and the others are blocked at any time. In that case, the voltage source can be regarded as a quasi-dc source practically. Then, the PWM inverter and the motor load are modeled as a current source $(i_{\rm inv})$, which represents the mean current flowing from the dc-link to the inverter during a PWM period. L_s and R_s are the equivalent series impedance of the input power source including the input filter, and $C_{\rm dc}$ is the dc-link capacitance. The state equations of the system shown in Fig. 1 are described by

$$L_s \frac{di_s}{dt} = v_s - R_s i_s - v_{\rm dc} \tag{1}$$

$$C_{\rm dc} \frac{dv_{\rm dc}}{dt} = i_s - i_{\rm inv}. \tag{2}$$

If the motor load pulls a constant power of P_L, the inverter current $i_{\rm inv}$ can be expressed as

$$i_{\rm inv} = P_L / v_{\rm dc} = \frac{P_L}{v_{\rm dc0} + \widetilde{v}_{\rm dc}} \tag{3}$$

where $v_{\rm dc0}$ is a mean value of the dc-link voltage and $\widetilde{v}_{\rm dc}$ is a dc-link voltage deviation. If $\widetilde{v}_{\rm dc}$ is relatively small compared to its mean value, the inverter current can be linearized as

$$i_{\rm inv} = \frac{P_L}{v_{\rm dc0} + \widetilde{v}_{\rm dc}} \cong \frac{P_L}{v_{\rm dc0}} - \frac{P_L}{v_{\rm dc0}^2}\widetilde{v}_{\rm dc}. \tag{4}$$

From (4), it can be shown that the CPL acts as a negative impedance. With the linearized inverter current in (4), the state equations of (1) and (2) have the following characteristic equation:

$$s^2 + \left(\frac{R_s}{L_s} - \frac{P_L}{C_{\rm dc}v_{\rm dc0}^2}\right)s + \left(\frac{v_{\rm dc0}^2 - R_sP_L}{L_sC_{\rm dc}v_{\rm dc0}^2}\right) = 0. \tag{5}$$

From (5), the stability criterion for the dc-link capacitor can be obtained as

$$C_{\rm dc} > \frac{L_sP_L}{R_sv_{\rm dc0}^2}. \tag{6}$$

It can be noted that the generating systems are inherently stable even though the dc-link capacitor is extremely reduced since P_L is negative in generating applications. In motoring applications, however, if the capacitance of the inverter does not satisfy the criterion in (6), the states of the system including the dc-link voltage and the source current are unstable or oscillating [10], [13]. If the electrolytic capacitor at the dc-link is replaced with a film capacitor with small capacitance, it is hardly possible for the system to meet this criterion. As a result, the semiconductor switches such as IGBTs may be destroyed from overvoltage. In order to prevent this situation, a special algorithm to stabilize the dc-link voltage is required if the dc-link capacitance is not sufficiently large. The proposed stabilization method used to solve this problem will be explained in the next section.

III. Proposed Stabilization Method

The dc-link instability problem previously discussed can be solved by manipulating the inverter output current $(i_{\rm inv})$ according to the dc-link voltage fluctuation. One of the means of manipulating the inverter output current is to modify the torque-producing current command according to the dc-link voltage deviation since the torque of the motor is proportional to the output power. However, if the oscillation frequency, which is related to the system parameters of the input inductance and the dc-link capacitance, is too high for the current controller to generate the manipulating current, the instability of the system does not disappear even by manipulating the torque-producing current command. Generally, the resonance frequency of the system with reduced dc-link capacitor is quite higher than the current control bandwidth because the frequency is in inverse proportion to the square root of the dc-link capacitance. Therefore, manipulating the voltage command of the inverter is more effective than manipulating the torque-producing current command for suppressing the high frequency oscillation.

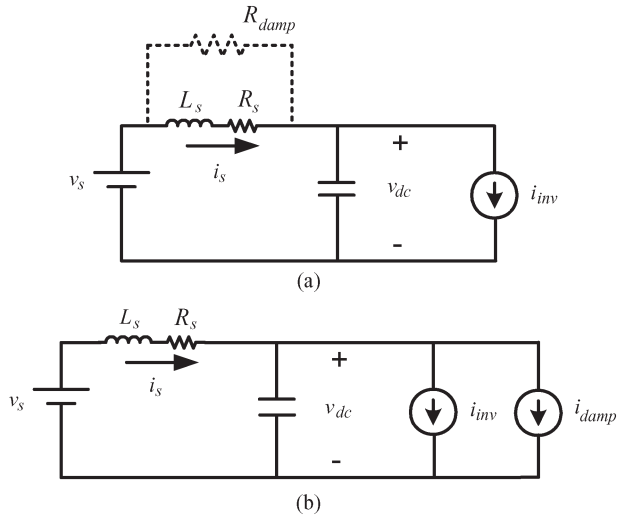

Fig. 2. (a) Virtual resistor $(R_{\rm damp})$ to stabilize the voltage of the dc-link capacitor. (b) Implementation of the virtual resistance by adding the damping current $(i_{\rm damp})$.

A. DC-Link Voltage Stabilization Method for CPL

The basic principle of the proposed stabilization is that the negative impedance of the CPL can be neutralized by adding some positive impedance (or damping). As shown in Fig. 2(a), a virtual damping resistor is added between the voltage source and the dc-link capacitor in order to increase the damping of the system. Since the virtual damping resistor is not a physical one, the losses owing to the damping are generated not at the virtual damping resistor but at the motor and the inverter because the real damping current flows through the inverter and the motor. The implementation of the active damping effect using the virtual damping resistor can be achieved by injecting additional inverter current $(i_{\rm damp})$ as shown in Fig. 2(b), which is proportional to the difference between the dc-link voltage and the estimated source voltage as

$$i_{\rm damp} = \frac{(v_{\rm dc} - \hat{v}_s)}{R_{\rm damp}} \tag{7}$$

where $\hat{v}_s$ is the estimated source voltage. The estimation of the source voltage will be explained in Section III-B. Because the total currents seen from the dc-link capacitor look exactly the same as if a physical resistor is connected to the dc-link, the oscillation of the dc-link voltage can be effectively damped. As $R_{\rm damp}$ decreases, the dc-link voltage is tightly regulated to the source voltage. In other words, the oscillation of the dc-link voltage is suppressed more and more by selecting a smaller damping resistance. However, a larger damping current requires a larger inverter voltage, so it is recommended to set $R_{\rm damp}$ to be small enough just to prevent the instability of the system. The maximum value of $R_{\rm damp}$ which can stabilize the system can be calculated from the modified state equations where the damping current is added to the state equation in (2). By replacing $i_{\rm inv}$ in (2) with $i_{\rm inv} + i_{\rm damp}$, the modified state equation becomes

$$\begin{aligned} C_{\rm dc}\frac{dv_{\rm dc}}{dt} &= i_s - i_{\rm inv} - i_{\rm damp} \\ &= i_s - i_{\rm inv} - \frac{(v_{\rm dc} - \hat{v}_s)}{R_{\rm damp}}. \end{aligned} \tag{8}$$

In (8), the dc-link voltage deviation $\widetilde{v}_{\rm dc} = v_{\rm dc} - v_{\rm dc0}$, and the mean value of the dc-link voltage $v_{\rm dc0} \cong \hat{v}_s$ neglecting the source resistance, which is typically quite small. Then, using the linearized inverter current $i_{\rm inv}$ in (4), the modified state equation (8) yields

$$C_{\rm dc}\frac{dv_{\rm dc}}{dt} = i_s - \frac{P_L}{v_{\rm dc0}} + \frac{P_L}{v_{\rm dc0}^2}\widetilde{v}_{\rm dc} - \frac{\widetilde{v}_{\rm dc}}{R_{\rm damp}}. \tag{9}$$

Using (1) and (9), a new characteristic equation of the stabilized system can be calculated as

$$s^2 + \left(\frac{R_s}{L_s} - \frac{P_L}{C_{\rm dc}v_{\rm dc0}^2} + \frac{1}{C_{\rm dc}R_{\rm damp}}\right)s + \left(\frac{R_{\rm damp}v_{\rm dc0}^2 - R_{\rm damp}R_sP_L + R_sv_{\rm dc0}^2}{L_sC_{\rm dc}R_{\rm damp}v_{\rm dc0}}\right) = 0. \tag{10}$$

From the characteristic equation in (10), a stability condition is derived as follows:

$$\frac{1}{R_{\rm damp}} > \frac{P_L}{v_{\rm dc0}^2} - \frac{R_sC_{\rm dc}}{L_s}. \tag{11}$$

It can be concluded from (11) that the maximum damping resistance (or minimum damping admittance) becomes larger as the load power increases. That means that the dc-link voltage should be more tightly regulated with a smaller damping resistance as the load power increases. In addition, it can be also concluded that no damping resistance is required if the right side of (11) is negative since $R_{\rm damp}$ can be infinitely large in such cases. That is exactly the same conclusion that the system which meets the criteria in (6) is inherently stable.

After selecting an adequate damping resistance for the stabilization, the next implementation step is to realize the damping current $(i_{\rm damp})$ obtained from (7). Injection of the additional damping current $(i_{\rm damp})$ to the load machine can be achieved by adding an additional voltage vector $\vec{v}_{\rm damp}$ to the original voltage command vector $\vec{v}_{dq}^{\omega^*}$ from the current controller for the motor control. The damping voltage vector $\vec{v}_{\rm damp}$ which produces the damping current $(i_{\rm damp})$ can be directly calculated from the following equation since the output power of the inverter is equal to the inner product of the inverter voltage vector and the motor current vector:

$$i_{\rm damp} = \frac{3}{2}\frac{\vec{v}_{\rm damp}\cdot\vec{i}_{dq}^{\omega}}{v_{\rm dc}} \tag{12}$$

where $\vec{i}_{dq}^{\omega}$ is the motor current vector in the $d-q$ rotating reference frame.

There are infinite solutions of $\vec{v}_{\rm damp}$ in (12) because the equation is not a scalar equation but a 2-D vector equation. The solutions lie on the line which is vertical to the current vector $\vec{i}_{dq}^{\omega}$, as shown in Fig. 3(a). The best solution is the vector that has the least magnitude because $\vec{v}_{\rm damp}$ is to be added to the current controller output and it is basically a voltage disturbance to the current controller. Thus, the damping voltage vector $\vec{v}_{\rm damp}$ on the axis where the load current vector lies becomes the optimal solution. Because the solution vector lies on the load current vector, it is convenient to introduce a new reference frame

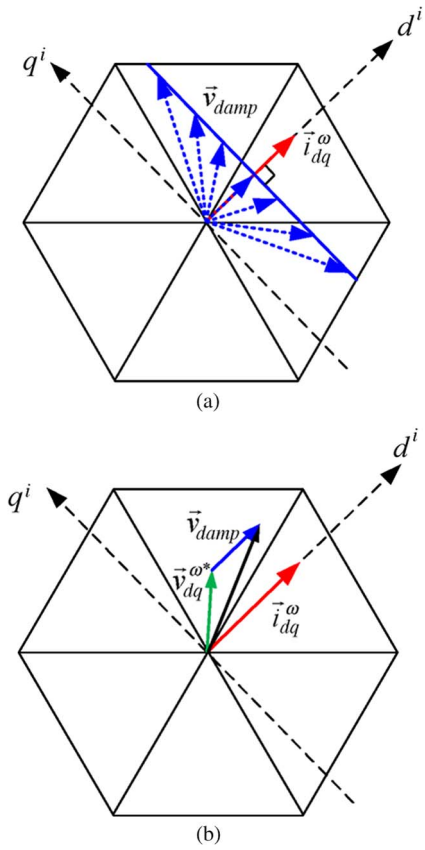

Fig. 3. (a) Several voltage vectors (blue) that produce the same damping current $(i_{\rm damp})$ with the motor current vector (red). (b) Space vector diagram of the voltage output of the inverter which is composed of the original voltage vector (green), the damping voltage vector (blue), and the final voltage output vector (black).

called load current reference frame where all load currents lie on the d-axis of the frame. Then, in the load current reference frame, the vector equation (12) can be transformed to a scalar equation as

$$v_{\rm damp}^i = \frac{2}{3}\frac{v_{\rm dc}i_{\rm damp}}{i_{\rm load}} = \frac{2}{3}\frac{v_{\rm dc}(v_{\rm dc} - \hat{v}_s)}{i_{\rm load}R_{\rm damp}} \tag{13}$$

where $i_{\rm load} = |\vec{i}_{dq}^{\omega}|$ is the magnitude of the load current and the superscript i means the load current reference frame.

After the additional damping voltage to inject is calculated from (13), it is added to the original voltage command from the current controller as shown in Fig. 3(b). The block diagram of the proposed stabilization algorithm is depicted in Fig. 4. In Fig. 4, there are two transformation blocks used to change the reference frame of the voltage command vectors. The first one rotates the reference frame from the synchronous reference frame to the current reference frame. Since the damping voltage is calculated in the current reference frame and it has only the d-axis component of the current reference frame, it is added to the d-axis voltage command from the current controller in the current reference frame. The second frame transformation finally rotates the reference frame from the current reference frame to the stationary reference frame for the PWM of the inverter.

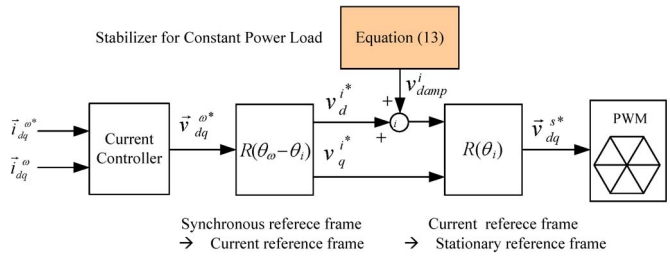

Fig. 4. Reference frame transformation incorporated with the proposed dc-link stabilization algorithm.

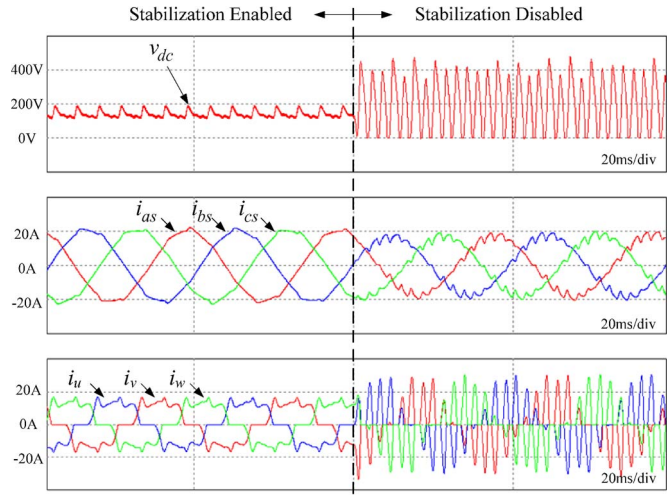

Fig. 5. Simulation results of dc-link voltage stabilization: dc-link voltage, motor currents, and source currents (from top to bottom).

TABLE I
PARAMETERS OF THE DRIVE SYSTEM

Parameter	Values
Rated power	1.8 kW
dc-link capacitance	9 μF
Filter inductance	1.5 mH
Grid voltage	110 Vrms
Grid frequency	60Hz
Rated speed	1500 r/min
Number of poles	4
Inductances (L_d / L_q)	3mH / 3mH
Resistance	0.5 Ω
Back-emf constant	0.101 V·s/rad

Fig. 5 shows the simulation results of the proposed stabilization algorithm. The simulation was performed with a permanent-magnet motor drive system, whose parameters are listed in Table I. Both the dc-link voltage and the source currents fluctuate significantly while the stabilization is disabled (right-half side of the waveform). With the proposed stabilization (left-half side of the waveform), both the dc-link voltage and the source currents are well stabilized, although the motor currents are a little distorted due to the added voltage $\vec{v}_{\rm damp}$ for stabilization. However, the motor currents are even more distorted while the stabilization is disabled because of significantly fluctuating dc-link voltage.

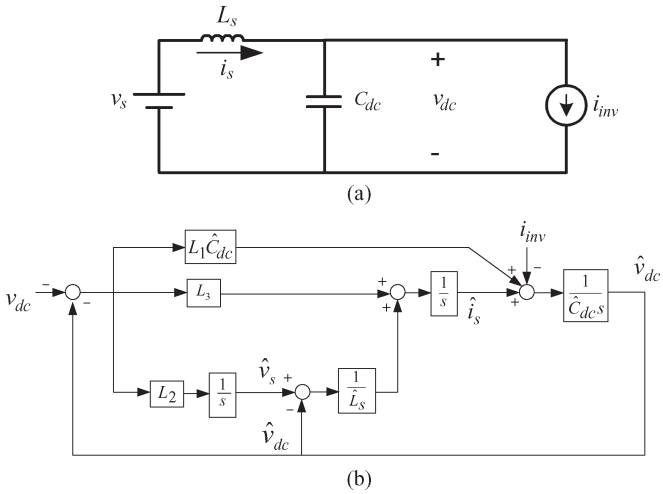

Fig. 6. (a) Simplified equivalent model for constructing a state estimator. (b) Block diagram of the proposed state estimator.

B. Source State Estimator

To achieve the active damping effect as shown in Fig. 2(a), it is required to obtain the dc-link voltage deviation due to the resonance. If the source voltage is pure dc, it is possible to obtain the dc-link voltage deviation by employing a high-pass filter or a bandpass filter at the dc-link voltage. However, if the source voltage is from a three-phase rectifier, it is not easy to distinguish the dc-link voltage deviation from the dc-link voltage containing the source voltage harmonics resulting from the rectification, since the resonance frequency is often close to the sixth harmonic frequency of the grid. Moreover, because the terminal voltage of the source includes the voltage drops due to internal impedance, it is difficult to measure the exact source voltage itself. Thus, a source state estimator is presented in order to estimate the source voltage. The purpose of this state estimator is to obtain both the source voltage and source current, which are necessary in stabilizing the system. From this state estimator, the dc-link voltage deviation due to the system instability, which is required to calculate the damping current in (7), is directly obtained by subtracting the estimated source voltage from the dc-link voltage.

In the system model depicted in Fig. 1, the states (voltage and current) of the source side can be estimated because the averaged inverter output current $(i_{\rm inv})$ is a known control variable and the system is completely observable. The averaged inverter current over one PWM period $(i_{\rm inv})$ can be directly calculated from the inverter voltage output $(\vec{v}^{\,\omega}_{dq})$ and the load (machine) current $(\vec{i}^{\,\omega}_{dq})$ as

$$i_{\rm inv} = \frac{3}{2}\frac{\vec{v}^{\,\omega}_{dq}\cdot\vec{i}^{\,\omega}_{dq}}{v_{\rm dc}}. \tag{14}$$

Neglecting the source resistance for simplicity, the system model is illustrated in Fig. 6(a), and the state-space system equation can be derived as

$$\begin{bmatrix}\dot{v}_{\rm dc}\\ \dot{v}_s\\ \dot{i}_s\end{bmatrix} = \begin{bmatrix}0 & 0 & \frac{1}{C_{\rm dc}}\\ 0 & 0 & 0\\ -\frac{1}{L_s} & \frac{1}{L_s} & 0\end{bmatrix}\begin{bmatrix}v_{\rm dc}\\ v_s\\ i_s\end{bmatrix} + \begin{bmatrix}-\frac{1}{C_{\rm dc}}\\ 0\\ 0\end{bmatrix} i_{\rm inv}. \tag{15}$$

Using the system model and the system input $(i_{\rm inv})$, it is possible to build a Luenberger-type estimator as shown in Fig. 6(b). The estimator equation is given by

$$\begin{bmatrix} \dot{\hat{v}}_{\rm dc} \\ \dot{\hat{v}}_s \\ \dot{\hat{i}}_s \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_{\rm dc}} \\ 0 & 0 & 0 \\ -\frac{1}{L_s} & \frac{1}{L_s} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{\rm dc} \\ \hat{v}_s \\ \hat{i}_s \end{bmatrix} + \begin{bmatrix} -\frac{1}{C_{\rm dc}} \\ 0 \\ 0 \end{bmatrix} i_{\rm inv} + \mathbf{L}\left[v_{\rm dc} - \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{\rm dc} \\ \hat{v}_s \\ \hat{i}_s \end{bmatrix} \right] \quad (16)$$

where $\mathbf{L} = \begin{bmatrix} L_1 \\ L_2 \\ L_3 \end{bmatrix}$ is the gain matrix of the estimator. The characteristic equation of the estimator with the gain matrix $\mathbf{L}$ is

$$s^3 + L_1 s^2 - \frac{1}{C_{\rm dc}}\left(L_3 + \frac{1}{L_s}\right) s + \frac{L_2}{C_{\rm dc} L_s} = 0. \quad (17)$$

The source state estimator should be much faster than the source voltage fluctuation in order to estimate the source voltage with least error. Thus, the bandwidth of the estimator should be much higher than six times the grid frequency (ω_g), since the source voltage seen from the dc-link has a lot of sixth harmonics. For example, all three poles are to be located on $s = -\omega_{bw} (\omega_{bw} \gg 6 \cdot \omega_g)$; then, the characteristic equation is equal to

$$(s + \omega_{bw})^3 = 0. \quad (18)$$

Since (17) and (18) should be identical, the gain matrix becomes

$$\mathbf{L} = \begin{bmatrix} 3\omega_{bw} \\ L_s C_{\rm dc} \omega_{bw}^3 \\ 3 C_{\rm dc} \omega_{bw}^2 - 1 \end{bmatrix}. \quad (19)$$

In the state estimator, only the dc-link voltage and load (motor) currents need to be measured, and both are prerequisite for conventional motor drive systems. Hence, the source voltage (v_s) and current (i_s) can be estimated without any additional measurement from the proposed estimator. The discrete-time prediction estimator derived from the continuous-time version is given in the Appendix.

C. DC-Link Voltage Stabilization Method for Rapid Load Change

From the source state estimator, the source current i_s, which cannot vary rapidly during one PWM period because of relatively large source inductance, can be estimated. Also, the inverter output current $i_{\rm inv}$ during the next PWM period is a known control variable from (14) assuming the load current $\vec{i}^{\,\omega}_{dq}[k] \cong \vec{i}^{\,\omega}_{dq}[k+1]$. Hence, it is possible to predict the dc-link capacitor current using the estimated source current and the inverter output current during the next PWM period. With this capacitor current, it is also possible to predict the dc-link voltage variation if the capacitance of the dc-link capacitor is known. Thus, the dc-link voltage variation during the next PWM period can be described as

$$\Delta v_{\rm dc}[k+1] = \frac{T}{\hat{C}_{\rm dc}} \left(\hat{i}_s[k+1] - i_{\rm inv}[k+1] \right) \quad (20)$$

where $\Delta v_{\rm dc}$ is the dc-link voltage variation after one control period T and $\hat{C}_{\rm dc}$ is the estimated dc-link capacitance.

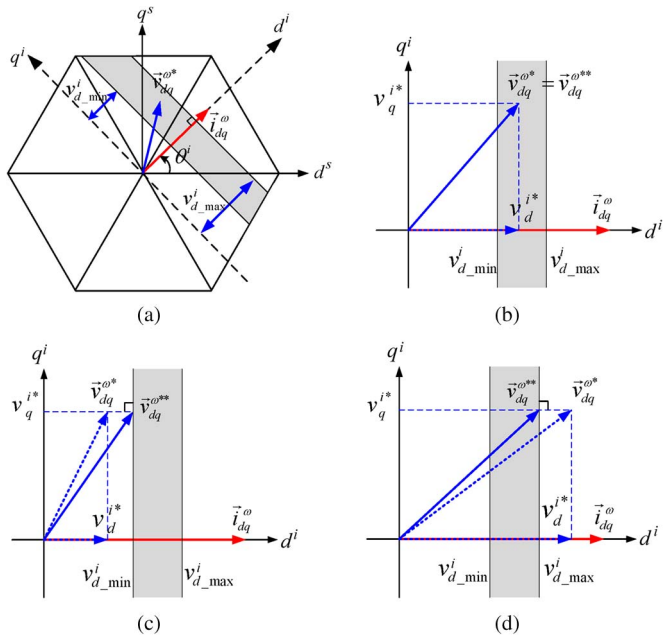

Fig. 7. (a) Allowable inverter voltage band (shaded) to avoid dc-link over-/undervoltage and a motor current vector (red). (b) Case I: the voltage command vector is on the band. (c) Case II (overvoltage): the d-axis voltage command is smaller than the lower limit. (d) Case III (undervoltage): the d-axis voltage command exceeds the upper limit.

Because the film capacitor has quite tight tolerance of capacitance less than 20% for its lifetime, the dc-link voltage variation can be predicted quite accurately as well. In other words, it is possible to regulate the dc-link voltage within a tolerable range by restricting the inverter output current $(i_{\rm inv})$ if the dc-link voltage could be out of the range during the transients such as rapid load changes. Because $i_{\rm inv}$ is the inner product of an output voltage vector and a load current vector, the allowable output voltage vectors which make the dc-link voltage bounded in a desired range can be represented as a band-shaped area of tolerable output voltage vector which is vertical to the load current vector on the voltage vector space as shown in Fig. 7(a). Therefore, the final voltage command vector should be on the band to avoid the dc-link over-/undervoltage. Thus, if the calculated voltage command vector is out of the band, the voltage vector should be moved into the band in order to make the dc-link voltage in an allowable range. To minimize the change in voltage output, the original voltage vector is projected on the boundary of the band, i.e., only the d-axis component in the load current reference frame is changed. If the upper and lower limits of the dc-link voltage are defined as $V_{\rm dc\_max}$ and $V_{\rm dc\_min}$, respectively, the criteria for the dc-link

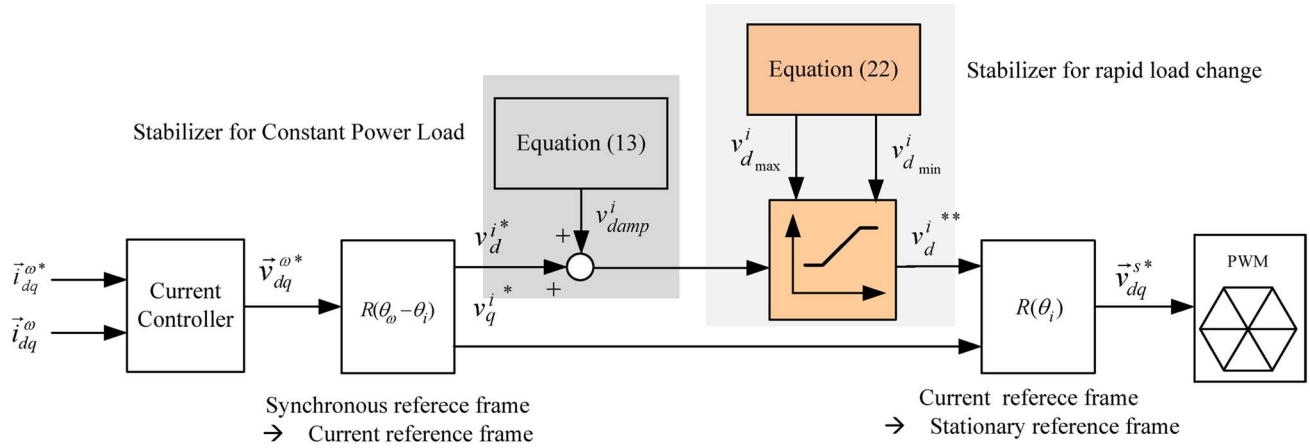

Fig. 8. Proposed dc-link stabilization algorithm implemented as a d-axis voltage limiter for suppressing the transient voltage fluctuation at the dc-link due to rapid load changes.

voltage to be between $V_{\mathrm{dc\_max}}$ and $V_{\mathrm{dc\_min}}$ can be calculated using (20) as

$$\begin{aligned} & v_d^i[k] i_d^i[k] \\ & \quad > \frac{2}{3} \hat{v}_{\mathrm{dc}}[k+1] \left\{ \hat{i}_s[k+1] - \frac{\hat{C}_{\mathrm{dc}}}{T} \left(V_{\mathrm{dc\_max}} - \hat{v}_{\mathrm{dc}}[k+1] \right) \right\} \\ & v_d^i[k] i_d^i[k] \\ & \quad < \frac{2}{3} \hat{v}_{\mathrm{dc}}[k+1] \left\{ \hat{i}_s[k+1] - \frac{\hat{C}_{\mathrm{dc}}}{T} \left(V_{\mathrm{dc\_min}} - \hat{v}_{\mathrm{dc}}[k+1] \right) \right\}. \end{aligned} \tag{21}$$

From (21), the lower limit $(v_{d\_\mathrm{min}}^i)$ and the upper limit $(v_{d\_\mathrm{max}}^i)$ of the d-axis voltage command in the load current reference frame can be obtained as

$$\begin{aligned} & v_{d\_\mathrm{min}}^i[k] \\ & \quad = \frac{2}{3} \frac{\hat{v}_{\mathrm{dc}}[k+1]}{i_d^i[k]} \left\{ \hat{i}_s[k+1] - \frac{\hat{C}_{\mathrm{dc}}}{T} \left(V_{\mathrm{dc\_max}} - \hat{v}_{\mathrm{dc}}[k+1] \right) \right\} \\ & v_{d\_\mathrm{max}}^i[k] \\ & \quad = \frac{2}{3} \frac{\hat{v}_{\mathrm{dc}}[k+1]}{i_d^i[k]} \left\{ \hat{i}_s[k+1] - \frac{\hat{C}_{\mathrm{dc}}}{T} \left(V_{\mathrm{dc\_min}} - \hat{v}_{\mathrm{dc}}[k+1] \right) \right\}. \end{aligned} \tag{22}$$

The limit values in (22) are calculated every sampling period from the estimated source current, dc-link voltage, and measured load current. Then, the d-axis voltage command in the load current reference frame is bounded by these limit values. Fig. 7(b)–(d) shows all possible situations. If the d-axis component of the original voltage command is between the limits as shown in Fig. 7(b), the dc-link voltage is expected to be between the predetermined levels ($V_{\mathrm{dc\_max}}$ and $V_{\mathrm{dc\_min}}$) at the next sampling period. Thus, the original voltage command can be applied to the motor without change. However, in the case of Fig. 7(c) and (d), the dc-link voltage is expected to be out of the dc-link voltage limits. Specifically, in the case of

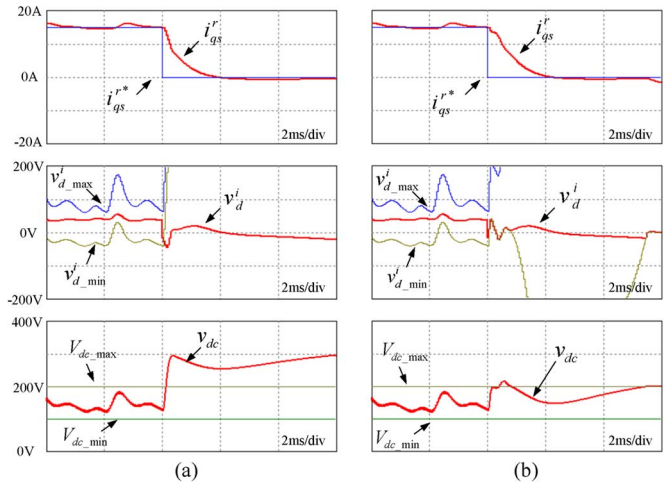

Fig. 9. Simulation results of dc-link voltage stabilization for rapid load change (step down): q-axis motor current command and response in rotor reference frame, d-axis voltages in load current reference frame, and dc-link voltage. (a) Without stabilization. (b) With the proposed stabilization method.

Fig. 7(c), the dc-link voltage will exceed $V_{\mathrm{dc\_max}}$ if the dotted original voltage command is applied to the motor since the d-axis voltage is smaller than $v_{d\_\mathrm{min}}^i$. Thus, the voltage command vector is projected on the lower boundary by limiting the d-axis voltage command by $v_{d\_\mathrm{min}}^i$. In the case of Fig. 7(d), on the other hand, the dc-link voltage will decrease below $V_{\mathrm{dc\_min}}$ since the d-axis voltage is larger than $v_{d\_\mathrm{max}}^i$. Hence, the voltage command vector is projected on the upper boundary by limiting the d-axis voltage command by $v_{d\_\mathrm{max}}^i$.

As a result, the dc-link voltage is guaranteed to be in the predetermined range after the d-axis voltage command in the load current reference frame is bounded by the limit values in (22) even with rapid load change. This algorithm can be implemented as a voltage limiter in the load current reference frame and is incorporated with the previously explained stabilization algorithm in Section III-A as shown in Fig. 8.

Figs. 9 and 10 show the simulation results of the proposed stabilization method for rapid load change. In Fig. 9, the q-axis motor current command in the rotor reference frame, which is the torque-producing current command, is changed to zero stepwise in order to cause overvoltage at the dc-link. Until the

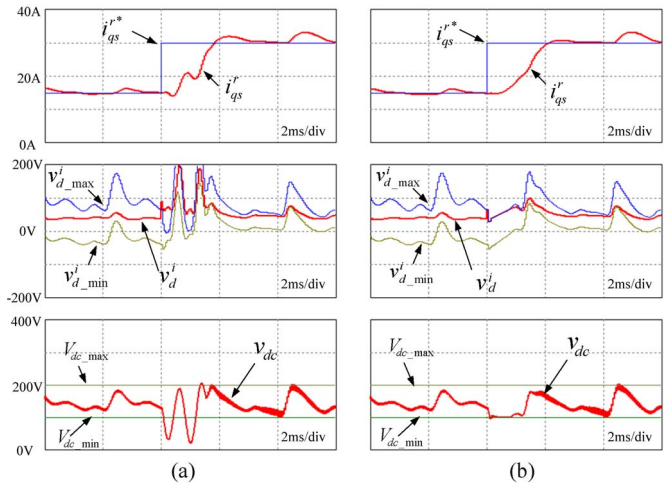

Fig. 10. Simulation results of dc-link voltage stabilization for rapid load change (step up): q-axis motor current command and response in rotor reference frame, d-axis voltages in load current reference frame, and dc-link voltage. (a) Without stabilization. (b) With the proposed stabilization method.

current command changes, the d-axis voltage v_d^i is between the upper limit $v_{d\_\max}^i$ and the lower limit $v_{d\_\min}^i$, corresponding to case I in Fig. 7(b). After the current reference changes to zero, the dc-link voltage increases rapidly in Fig. 9(a), where the proposed stabilization is disabled, and finally goes over $V_{\mathrm{dc}\_\max}$. This shows case II in Fig. 7(c) because the d-axis voltage v_d^i goes below the lower limit $v_{d\_\min}^i$. Once v_d^i goes out of the limit, $v_{d\_\min}^i$ rises even more in order to suppress the increase of the dc-link voltage. On the other hand, in Fig. 9(b), the dc-link voltage is well regulated since the d-axis voltage v_d^i is limited to $v_{d\_\min}^i$, although the current response is a little slowed down due to this action. On the contrary, the q-axis motor current command in the rotor reference frame steps up in the simulation shown in Fig. 10. In that case, the dc-link voltage in Fig. 10(a) decreases below $V_{\mathrm{dc}\_\min}$, where the proposed stabilization is disabled. This situation corresponds to case III in Fig. 7(d) because the d-axis voltage v_d^i goes over the upper limit $v_{d\_\max}^i$. With the proposed stabilization, the dc-link voltage does not decrease below $V_{\mathrm{dc}\_\min}$ because the d-axis voltage v_d^i is limited to $v_{d\_\max}^i$ as shown in Fig. 10(b).

IV. Experimental Results

The performances of the proposed dc-link stabilization algorithms are verified by experiments. The motor used in the experiment is a 2-kW permanent-magnet synchronous motor. The dc-link capacitance is 9 μF, and the per-phase inductance of the source is 1.5 mH. A three-phase 110-Vrms voltage source and a three-phase diode rectifier were used as a dc voltage source to dc-link. All of the proposed algorithms were implemented using a digital signal processor. An illustration of the experimental setup is shown in Fig. 11, and the detailed parameters of the system are listed in Table I.

Fig. 12 shows the performance of the proposed source state estimator for estimating the source current and voltage. The estimated source voltage in Fig. 9(b) is utilized to obtain the dc-link voltage deviation in (7), and the estimated source current

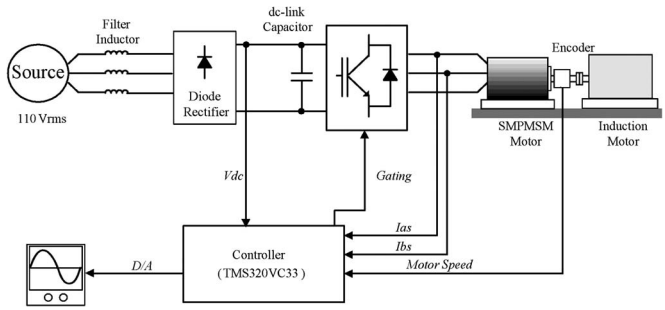

Fig. 11. Experiment hardware setup.

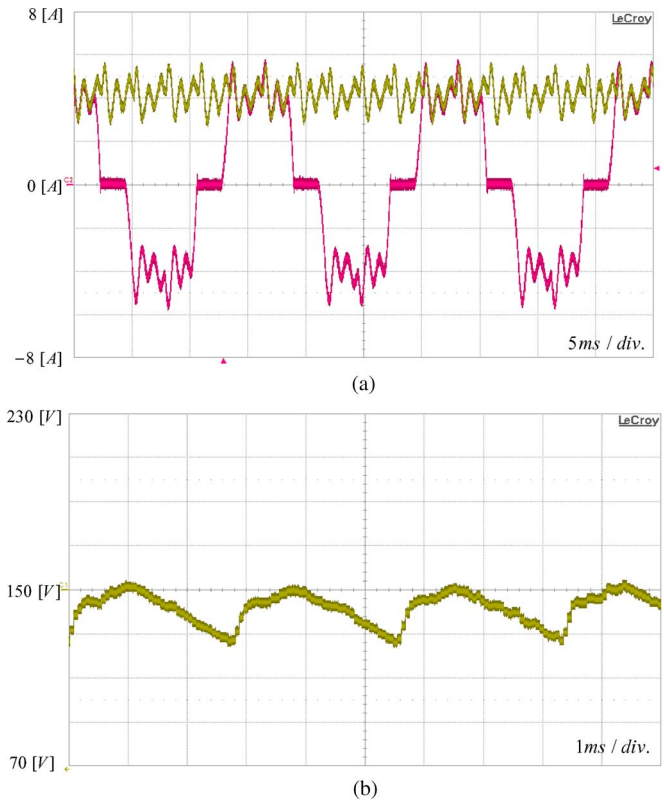

Fig. 12. Estimated source states from the proposed source state estimator. (a) Estimated source current (green) and measured source current (red). (b) Estimated source voltage (green).

in Fig. 9(a) is used to calculate the output voltage limits in (18), respectively. Since a three-phase diode rectifier was used as a power source, the estimated current tracks the positive envelope of the real source current. This is because the estimator regards the three-phase power source as a quasi-dc source as shown in Fig. 5(a). For the same reason, the estimated source voltage also looks like the rectified three-phase grid voltage. Since the proposed estimator estimates the source voltage accurately, the stabilization algorithm neglects the dc-link voltage fluctuation due to the rectification and responds only to the resonance.

To verify the proposed stabilization algorithm for CPL, the motor was accelerated with a constant torque. The waveforms of the q-axis motor current in rotor reference frame, motor speed, source current, and dc-link voltage during acceleration from zero speed are shown in Fig. 13. Without applying the

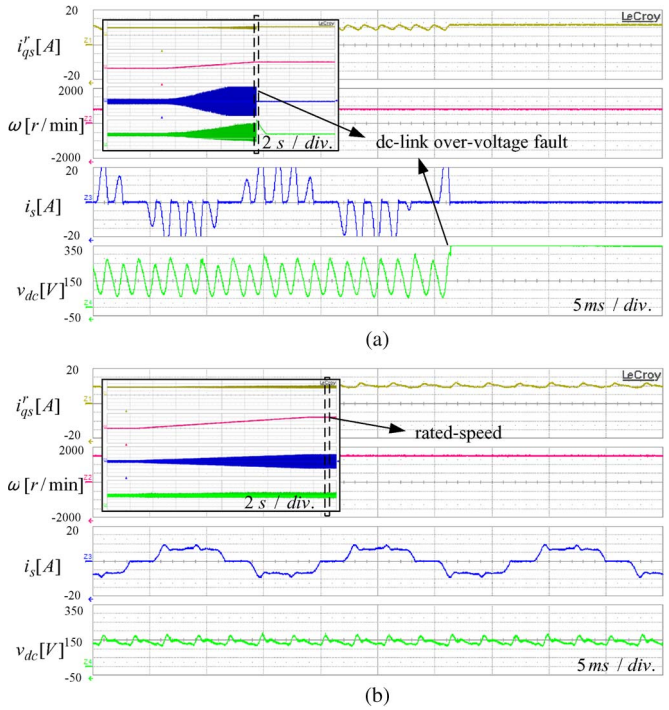

Fig. 13. Constant power output waveforms of the q-axis motor current in rotor reference frame, motor speed, source current, and dc-link voltage (from top to bottom). (a) Without stabilization. (b) With the proposed stabilization method in Section III-A.

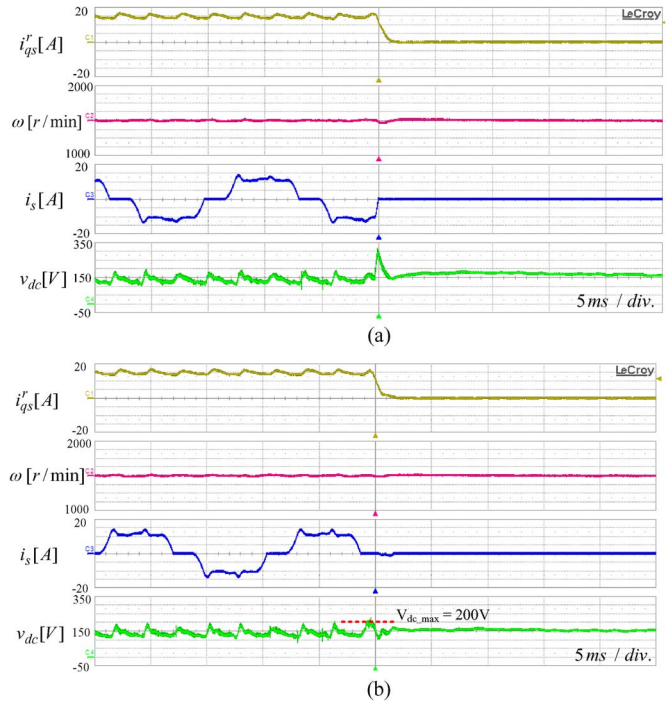

Fig. 14. Waveforms of the q-axis motor current in rotor reference frame, motor speed, source current, and dc-link voltage (from top to bottom) just after a step change in the motor torque. (a) Without stabilization. (b) With the proposed stabilization method in Section III-C.

proposed method, the inverter was stopped when the motor speed is about 800 r/min owing to the dc-link overvoltage fault as shown in Fig. 13(a), whereas the motor reached its rated speed of 1500 r/min with the proposed stabilization as shown in Fig. 13(b). In the waveforms in Fig. 13(a), the dc-link voltage and source current are significantly unstable and fluctuating. It can be deduced that the dc-link capacitance of the tested system is not enough to meet the stability criterion in (6). With the proposed stabilization method explained in Section III-A, both the source current and the dc-link voltage are well stabilized as shown in Fig. 13(b).

Fig. 14(a) shows the dc-link voltage spike over 100 V at the step load change of 50% of the rated power, and the spike results in overvoltage trip of the inverter. Of course, this voltage spike will be larger as the load power changes more rapidly. Fig. 14(b) shows the result at the same load change with the proposed algorithm proposed in Section III-C. Because the maximum voltage limit $(V_{\mathrm{dc\_max}})$ is set to 200 V, the dc-link voltage is limited by 200 V as shown in Fig. 14(b). Even though the proposed algorithm directly modifies the voltage output, it can be noted that the current response is a little affected by this algorithm. That is because the proposed algorithm works only for a negligibly short time when the rate of the load change is excessively large. As a result, it does not degrade the current control performance in normal operation.

V. Conclusion

Instability problem of the dc-link voltage has been known to be a severe problem for the reduced capacitor inverter. This paper has briefly reviewed the instability problems due to both the CPL and the rapid load change and has introduced novel stabilization methods to solve both problems.

The proposed algorithms are capable of stabilizing both the dc-link voltage and the source current by utilizing a closed-loop source state estimator which estimates both the source voltage and current. The proposed source state estimator makes the stabilization algorithm respond to the resonance only and not to the source voltage variation. Moreover, by directly manipulating the output voltage command, it is possible for the control law to take effect immediately. Thus, the dc-link voltage oscillation can be effectively suppressed even though the oscillation frequency is over the bandwidth of the current controller. The stabilization algorithm for the rapid load change utilizes the estimated source current in order to predict the dc-link voltage variation. As a result, the dc-link voltage is bounded by predetermined limits even in the case of rapid load change. Moreover, the method does not degrade the current controller performance during normal operations because it automatically works only while the dc-link voltage is predicted to be out of tolerable range. The experimental results verify that the proposed algorithms can successfully stabilize the dc-link voltage of the inverter.

Appendix [28]

From the continuous-time state-space equations in (15), the solution is evaluated by

$$\mathbf{x}(kT+T) = e^{\mathbf{A}T}\mathbf{x}(kT) + \int_0^T e^{\mathbf{A}\tau}d\tau\mathbf{B}i_{\mathrm{inv}}(kT) \qquad (23)$$

where

$$\mathbf{x}=\begin{bmatrix} v_{\rm dc} \\ v_s \\ i_s \end{bmatrix} \quad \mathbf{A}=\begin{bmatrix} 0 & 0 & \frac{1}{C_{\rm dc}} \\ 0 & 0 & 0 \\ -\frac{1}{L_s} & \frac{1}{L_s} & 0 \end{bmatrix} \quad \mathbf{B}=\begin{bmatrix} -\frac{1}{C_{\rm dc}} \\ 0 \\ 0 \end{bmatrix}$$

and T is the sampling period. If we define

$$\mathbf{\Phi}=e^{\mathbf{A}T} \tag{24}$$

$$\mathbf{\Gamma}=\int_0^T e^{\mathbf{A}\tau}d\tau\mathbf{B} \tag{25}$$

(23) yields a difference equation in standard form

$$\mathbf{x}[k+1]=\mathbf{\Phi}\mathbf{x}[k]+\mathbf{\Gamma}i_{\rm inv}[k]. \tag{26}$$

The series expansion of $e^{\mathbf{A}T}$ can be represented by series expansions

$$\begin{aligned}\mathbf{\Phi}&=e^{\mathbf{A}T}\\ &=\mathbf{I}+\mathbf{A}T+\frac{\mathbf{A}^2T^2}{2!}+\frac{\mathbf{A}^3T^3}{3!}+\frac{\mathbf{A}^4T^4}{4!}+\cdots\\ &=\mathbf{I}+\mathbf{A}T\mathbf{\Psi}\end{aligned} \tag{27}$$

where $\mathbf{\Psi}=\mathbf{I}+((\mathbf{A}T)/2!)+((\mathbf{A}^2T^2)/3!)+((\mathbf{A}^3T^3)/4!)+\cdots$.

The integral in (25) yields

$$\begin{aligned}\mathbf{\Gamma}&=\int_0^T e^{\mathbf{A}\tau}d\tau\mathbf{B}\\ &=\sum_{k=0}^{\infty}\frac{\mathbf{A}^kT^{k+1}}{(k+1)!}\mathbf{B}\\ &=\mathbf{\Psi}T\mathbf{B}.\end{aligned} \tag{28}$$

Since $\mathbf{A}^3=-(1/(L_sC_{\rm dc}))\mathbf{A}$, the infinite series $\mathbf{\Psi}$ can be evaluated to give

$$\begin{aligned}\mathbf{\Psi}&=\mathbf{I}+\frac{\mathbf{A}T}{2!}+\frac{\mathbf{A}^2T^2}{3!}+\frac{\mathbf{A}^3T^3}{4!}\cdots\\ &=\mathbf{I}+\frac{L_sC_{\rm dc}}{T}\left(1-\cos\frac{T}{\sqrt{L_sC_{\rm dc}}}\right)\mathbf{A}\\ &\quad+L_sC_{\rm dc}\left(1-\frac{\sqrt{L_sC_{\rm dc}}}{T}\sin\frac{T}{\sqrt{L_sC_{\rm dc}}}\right)\mathbf{A}^2.\end{aligned} \tag{29}$$

Substituting $\mathbf{\Psi}$ in (27) and (28), the discrete-time state-space matrices are obtained

$$\mathbf{\Phi}=\begin{bmatrix} \cos\frac{T}{\sqrt{L_sC_{\rm dc}}} & 1-\cos\frac{T}{\sqrt{L_sC_{\rm dc}}} & \sqrt{\frac{L_s}{C_{\rm dc}}}\sin\frac{T}{\sqrt{L_sC_{\rm dc}}} \\ 0 & 1 & 0 \\ -\sqrt{\frac{C_{\rm dc}}{L_s}}\sin\frac{T}{\sqrt{L_sC_{\rm dc}}} & \sqrt{\frac{C_{\rm dc}}{L_s}}\sin\frac{T}{\sqrt{L_sC_{\rm dc}}} & \cos\frac{T}{\sqrt{L_sC_{\rm dc}}} \end{bmatrix}$$

$$\mathbf{\Gamma}=\begin{bmatrix} -\sqrt{\frac{L_f}{C_{\rm dc}}}\sin\frac{T}{\sqrt{L_sC_{\rm dc}}} \\ 0 \\ 1-\cos\frac{T}{\sqrt{L_sC_{\rm dc}}} \end{bmatrix}. \tag{30}$$

Using the discrete-time state-space equation, the closed-loop prediction estimator can be constructed as follows:

$$\hat{\mathbf{x}}[k+1]=\mathbf{\Phi}\hat{\mathbf{x}}[k]+\mathbf{\Gamma}i_{\rm inv}[k]+\mathbf{L}\left[v_{\rm dc}[k]-\hat{v}_{\rm dc}[k]\right] \tag{31}$$

where $\mathbf{L}=\begin{bmatrix} L_1 \\ L_2 \\ L_3 \end{bmatrix}$ is the estimator gain matrix. To design the value of $\mathbf{L}$, it is necessary to specify the desired pole locations in z-domain to obtain the desired estimator characteristic equation, which is represented by

$$\det\left|z\mathbf{I}-\mathbf{\Phi}+\mathbf{L}[1\quad 0\quad 0]\right|=0. \tag{32}$$

If we set the pole locations in s-domain as s_1, s_2, and s_3, the equivalent poles in z-domain z_1, z_2, and z_3 can be computed by using the relationship $z=e^{sT}$. Finally, the gain matrix $\mathbf{L}$ is calculated by pole-placement method using (32) and the desired characteristic equation

$$(z-z_1)(z-z_2)(z-z_3)=0. \tag{33}$$

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