Asymmetric Control of DC-Link Voltages for Separate MPPTs in Three-Level Inverters

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***Abstract*—It is important to improve the overall efficiency of a photovoltaic (PV) inverter when it is connected to the grid. Fundamentally, the conversion efficiency from dc to ac power of an inverter is important. However, in the presence of partial shading, maximum power point tracking (MPPT) on PV modules is more important than the conversion efficiency. In this paper, a new control method for a three-level inverter is proposed. With the proposed method, each dc-link voltage of the three-level inverter can be asymmetrically regulated. When PV modules are split into two and each split module is connected to the respective dc-link capacitors of the inverter, the asymmetric control can be helpful because separate MPPTs are possible. The effectiveness of the proposed method was examined through experiments with a T-type three-level inverter, where each dc-link capacitor was supplied by a PV simulator emulating two separate PV modules under different shading conditions.**

***Index Terms*—Asymmetric voltage control, grid-connected inverter, maximum power point tracking (MPPT), photovoltaic (PV), three-level inverter.**

I. Introduction

CURRENTLY, the use of renewable energy is gaining increased amounts of attention due to environmental issues. Moreover, while the cost of the fossil fuels has increased, the cost of photovoltaic (PV) generation has decreased. Therefore, PV generation is becoming a viable solution in the event of an energy crisis. For example, multimegawatt PV plants are common in many places [1]–[3].

There are many topologies for connecting PV modules to the grid [4]. Among these, the centralized inverter is preferred in large-scale PV applications for practical reasons [3]. However, in terms of maximum power point tracking (MPPT), the centralized inverter may not be the best topology with which to maximize the power generation, as all of the PV modules are rigidly tied to a single inverter [5]. It would be desirable to consider the mismatches in PV modules [21].

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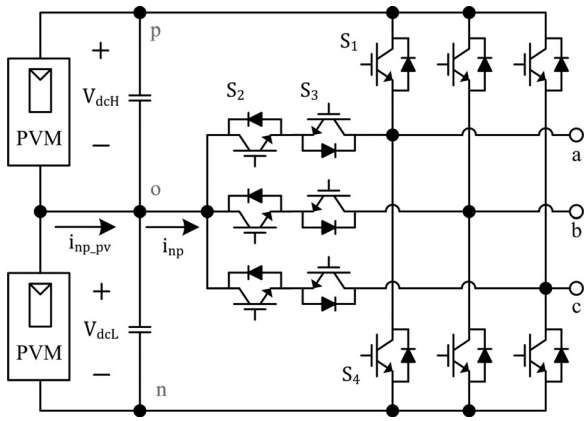

Fig. 1. PV modules and the T-type three-level PV inverter.

For better MPPT, additional dc–dc converters can be used to connect split PV modules to the centralized inverter [4], [6], [22]. However, although this structure may be helpful to deal with partial shade, the conversion efficiency may be degraded due to multiple conversions. Moreover, the installation and maintenance costs increase. Therefore, it is worth augmenting the degree of freedom for MPPT while the number of conversion stages does not increase.

Recently, three-level inverters have been discussed for implementing a centralized PV inverter, as the conversion efficiency can be increased by reducing switching losses and the output harmonic property can be improved. In particular, the T-type three-level inverter shown in Fig. 1 is preferred because conduction losses are further minimized by reducing the average number of switch modules on the current paths [7]. Inherently, the three-level inverter has a split dc-link, whose voltages can be controlled by manipulating the zero-sequence voltage added to the voltage references. Although the voltages of the split dc-link are supposed to be symmetric in general [8]–[11], [17], [18], they can be regulated asymmetrically. At the same time, as shown in Fig. 1, the current path of $i_{\mathrm{np\_pv}}$ can be intentionally established. Then, if the asymmetric regulation applies to the split PV connection in Fig. 1, separate MPPTs on the PV modules become possible without an increment in the conversion stage.

Several attempts to control dc-link voltages asymmetrically in multilevel inverters have been reported [12]–[14]. They can be differentiated according to their pulsewidth modulation (PWM) schemes.

The asymmetric control of the split dc-link based on direct power control (DPC) has been reported [12], [13]. Because

the DPC method is based on variable switching frequency, the filter design cannot easily meet the harmonic and EMI regulations [15], [16], [23], [24]. Moreover, as described in [12], the switching frequency of an inverter based on DPC should be high enough to achieve a tolerable quality of the grid currents, thus resulting in higher switching losses [25]. Other method based on space vector modulation (SVM) has been reported for the asymmetric control [14]. Intrinsically, the SVM method is complicated to implement because the dwell time of each vector should be geometrically computed. In addition, the sector in which the voltage vector is included should be identified and an extra table is required to optimize the switching patterns [9], [10]. Moreover, additional compensation should be considered to handle asymmetric dc-link voltages [11]. Even with this compensation, the switching frequency can be intermittently increased depending on the operating condition. This is not desirable for both the filter design and the loss minimization.

Compared to the SVM method, the carrier-based PWM method is simple to implement [17], [18]. Furthermore, the switching frequency of the inverter is fixed by the carrier-wave, as every switching state is changed only at the point where a reference intersects with the carrier. Using the carrier-based PWM method, the asymmetric control of the split dc-link can be easily implemented. This paper details how the zero-sequence voltage can be exploited for the asymmetric control. In Section II, the overall control structures are delineated with their control gains. Section III describes how the neutral point current in the inverter is changed by the zero-sequence voltage. After the proposed method is assessed via experimental results in Section IV, the conclusions are given in Section V.

II. Controllers for Asymmetric DC-link Voltages

A. Voltage Control of a Split DC-Link

The voltages of a split dc-link in a three-level inverter can be described as

$$\begin{cases} V_{\mathrm{dcH}} + V_{\mathrm{dcL}} = V_{\mathrm{dc}} \\ V_{\mathrm{dcH}} - V_{\mathrm{dcL}} = \delta V_{\mathrm{dc}} \end{cases} \tag{1}$$

where V_{dcH} and V_{dcL} are defined in Fig. 1.

Initially, the regulation of V_{dc} is conceptually equivalent to modulating the total energy stored in the capacitor bank of the inverter. That is, V_{dc} can be changed by regulating the active power supplied to the grid. For instance, if the output power to the grid is less than the input power from the PV modules, V_{dc} increases and vice versa. Therefore, regulating V_{dc} is easily achieved by the conventional method shown in Fig. 2. Each PI gain can be determined according to the method presented in earlier work [19].

On the other hand, the regulation of δV_{dc}, which is the difference between the high- and low-side dc-link voltages, is related to modulating the ratio between the output power from each capacitor. This can be described as

$$P_o = \frac{d}{dt} \times \frac{C_{\mathrm{dc}}}{2}(V_{\mathrm{dcH}}^2 + V_{\mathrm{dcL}}^2) \tag{2}$$

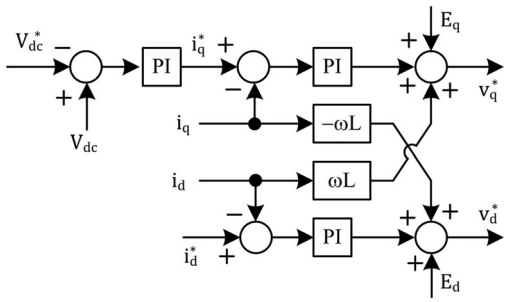

Fig. 2. Voltage controller for V_{dc}.

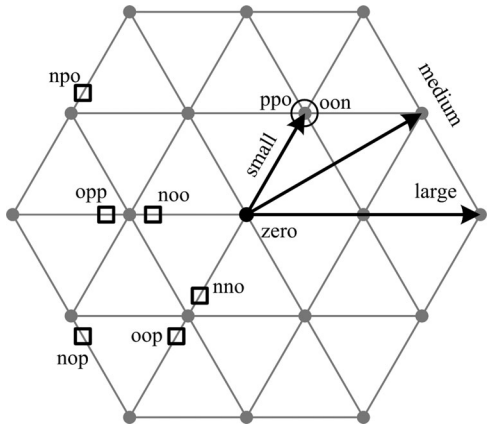

Fig. 3. Voltage vectors in the three-level inverter.

where P_o is the output power from the capacitor bank and C_{dc} is the high- or low-side capacitance of the split dc-link.

Given that the power from each dc-link is proportional to the corresponding voltage, the voltage difference can be adjusted by modulating the output power ratio between each dc-link. In addition, this modulation may be essential if asymmetric powers are supplied to the split dc-link from the PV modules, which are connected as shown in Fig. 1. According to (1), the simultaneous regulation of V_{dc} and δV_{dc} is equivalent to that of V_{dcH} and V_{dcL}. That is, when the references to V_{dcH} and V_{dcL} are given by separate MPPTs, these references can be achieved through the simultaneous regulation of V_{dc} and δV_{dc}. Particularly, how to regulate δV_{dc} is proposed in this paper.

B. Modifying PWM Under Asymmetric DC-link Voltages

The pole voltages of three-level inverters can be transformed into voltage vectors by means of Clarke transformation in the voltage vector plane. These vectors correspond to symmetric vertexes in Fig. 3 and can be classified as zero, small, medium, and large vectors according to their magnitude. Among them, the zero and small vectors are characterized by the overlap property [8]–[10].

In order to understand the overlap property, the indicator of "ppo" in Fig. 3 should be explained first. Here, "ppo" means that the voltage potentials of the a-, b-, and c-phase terminals are sequentially "p," "p," and "o when all potentials are defined as "p," "o," and "n" (see Fig. 1). Although the voltage vector of "ppo" corresponds to a small vector, the vector of "oon" also

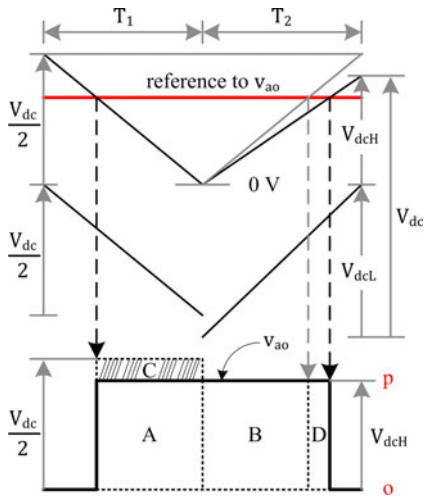

Fig. 4. Modification of carrier waves under asymmetric voltages.

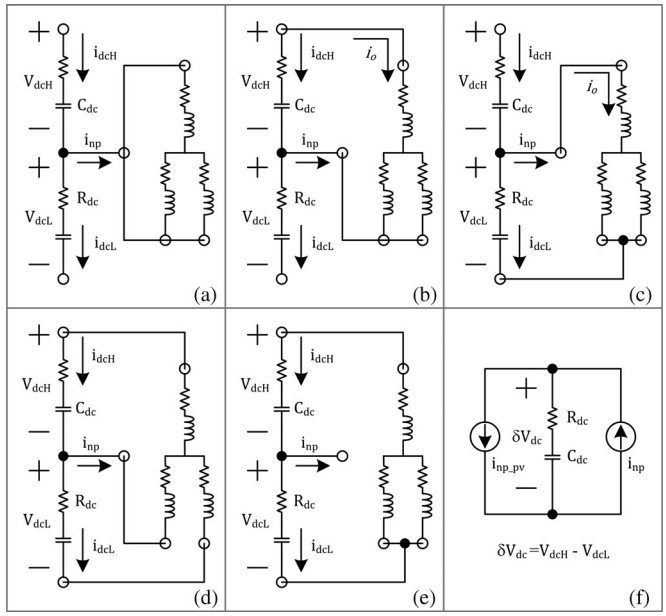

Fig. 5. Topological example circuits for each voltage vector and equivalent circuit for $\delta V_{\rm dc}$: (a) zero vector, (b) high-side small vector, (c) low-side small vector, (d) medium vector, (e) large vector, and (f) equivalent circuit for $\delta V_{\rm dc}$ based on(5).

coincides with that in the voltage vector plane. However, this overlap property of small vectors may be observed only if the dc-link voltages are symmetric.

For instance, when the ratio between $V_{\rm dcH}$ and $V_{\rm dcL}$ is 6:4, the positions of some voltage vectors are indicated by small squares in Fig. 3. In this case, the vectors of "opp" and "noo," which are supposed to be overlapped under the symmetric voltages, deviate from each other. Furthermore, the position of the medium vectors "npo" and "nop" shift as well. Therefore, the asymmetry of the dc-link should be considered in the PWM scheme to offset the shifting voltage vectors.

As shown in Fig. 4, two level-shifted carriers are required for carrier-based PWM in three-level inverters. To use the a-phase leg as an example, the high-side carrier is involved in setting the dwell time for switch $\rm S_1$ in Fig. 1 and the low-side carrier does so for $\rm S_2$. The switching operations of $\rm S_3$ and $\rm S_4$ are complementary to those of $\rm S_1$ and $\rm S_2$, respectively.

In Fig. 4, the terminal voltage of v_{ao}, which is the voltage from "o" to "a" (see Fig. 1), is depicted to discuss the effect of modifying PWM. Initially, when only the interval of T_1 in Fig. 4 is considered, each carrier height is assumed to be symmetric as usual, although the actual ratio between $V_{\rm dcH}$ and $V_{\rm dcL}$ is assumed to be 5:7. After the reference to $v_{\rm ao}$ is above the high-side carrier, $\rm S_1$ is turned ON. Additionally, the potential of "p" is connected to the a-phase when this occurs. Initially, the intended volt-second output during T_1 is the area sum of A and C (the hatched area), as the potential "p" is assumed to be $V_{\rm dc}/2$, which is half of $V_{\rm dc}$. However, because the actual potential of "p" is $V_{\rm dcH}$, which is the voltage of the high-side capacitor in Fig. 1, the actual volt-second output only includes the area A. That is, the amount of the area C is lost during T_1 because PWM is based on symmetric carriers. Meanwhile, $\rm S_2$ is fully turned ON because the reference is always above the low-side carrier in Fig. 4. However, the low-side carrier does not distort the volt-second output because the reference is positive.

To offset the volt-second loss, the peak-to-peak amplitude of each carrier can be simply modified as shown in the interval of T_2. Namely, the amplitudes of the high- and low-side carriers were set to $V_{\rm dcH}$ and $V_{\rm dcL}$, respectively. Then, compared to the case of T_1, the turn-on time of $\rm S_1$ increases under the same reference such that the volt-second output corresponds to the area sum of B and D, which is equal to that of A and C. That is, the actual output voltage during T_2 becomes equal to its reference in average sense. Similarly, it can be inferred that the effect of modifying the low-side carrier would arise if the reference is negative. Therefore, this modification of PWM is conducted so that the carrier waves reflect the actual split dc link voltages,$V_{\rm dcH}$ and $V_{\rm dcL}$, in real time.

C. Modeling of an Equivalent Circuit for $\delta V_{\rm dc}$ Control

A typical example of the topological circuit for each voltage vector is depicted in Fig. 5 when a three-phase *R–L* load is connected to the inverter. Based on the topological circuits, how $\delta V_{\rm dc}$ changes according to the voltage vectors was analyzed. Initially, the voltage of each dc-link capacitor is expressed in terms of the corresponding current, as

$$V_{\rm dcH}(t) = V_{\rm dcH0} + R_{\rm dc}\cdot i_{\rm dcH}(t) + \frac{1}{C_{\rm dc}}\int_0^t i_{\rm dcH}(t)\,dt \quad \text{(3-a)}$$

$$V_{\rm dcL}(t) = V_{\rm dcL0} + R_{\rm dc}\cdot i_{\rm dcL}(t) + \frac{1}{C_{\rm dc}}\int_0^t i_{\rm dcL}(t)\,dt \quad \text{(3-b)}$$

where $V_{\rm dcH0}$ and $V_{\rm dcL0}$ are the initial voltages of the high- and low-side dc-link capacitors, respectively. $R_{\rm dc}$ is the equivalent series resistance, and $C_{\rm dc}$ is the capacitance of each dc-link.

In addition, Kirchhoff's current law (KCL) can be applied at the neutral point in Fig. 5 as

$$i_{\rm dcH}(t) - i_{\rm dcL}(t) = i_{\rm np}(t). \quad (4)$$

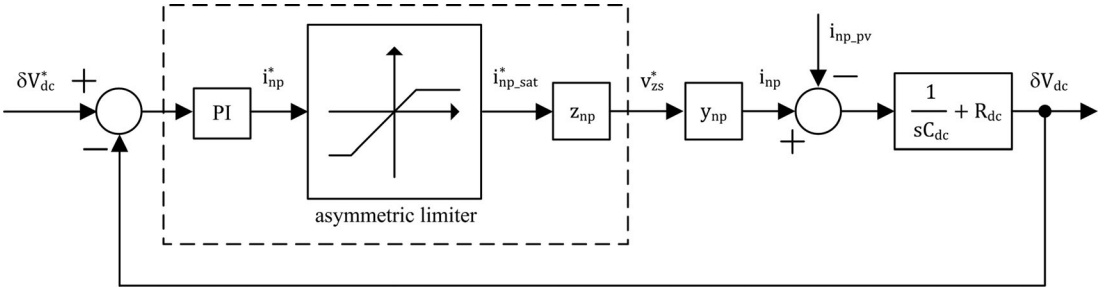

Fig. 6. Closed loop for the $\delta V_{\rm dc}$ control based on the equivalent circuit.

Based on the definitions in (1) and (4), $\delta V_{\rm dc}$ can be derived as (5) through the subtraction of (3-b) from (3-a)

$$\begin{aligned}\delta V_{\rm dc}\left(t\right) &= V_{\rm dcH}\left(t\right) - V_{\rm dcL}\left(t\right)\\ &= V_{\rm dcH0} - V_{\rm dcL0} + R_{\rm dc}\cdot i_{\rm np}\left(t\right)\\ &\quad + \frac{1}{C_{\rm dc}}\int_0^t i_{\rm np}\left(t\right)dt. \end{aligned} \tag{5}$$

That is, the neutral point current of $i_{\rm np}$, whose direction was defined in Fig. 1, corresponds to the current flowing into the equivalent capacitor, whose voltage is $\delta V_{\rm dc}$.

From (5), it can be inferred that the voltage difference $\delta V_{\rm dc}$ can be controlled by $i_{\rm np}$. When zero or large vectors are output, as shown in Fig. 5(a) and (e), $\delta V_{\rm dc}$ remains constant because $i_{\rm np}$ cannot flow. In contrast, small vectors can contribute to the variation of $\delta V_{\rm dc}$ and can be categorized into two types, as shown in Fig. 5(b) and (c), which are overlapped under the symmetric condition. Specifically, the load is only connected to the high-side capacitor under high-side small vectors, whereas this is also true for the low-side capacitor under low-side small vectors. When considering the relative directions of $i_{\rm np}$ to the same load current, as denoted by i_o, it is clear that each type of small vector leads to the opposite variation of $\delta V_{\rm dc}$ according to (5). Although medium vectors can alter $\delta V_{\rm dc}$ as shown in Fig. 5(d), they cannot serve as an alternative to each other in the carrier-based PWM method, unlike the small vectors that may be overlapped. Physically, it can be understood that modulating the zero-sequence voltage serves to determine which type of small vector is output more frequently.

Because PV modules are connected as proposed in Fig. 1, the neutral point current from the modules should be considered. This current of $i_{\rm np\_pv}$ can be considered as a shunt current source in the equivalent circuit shown in Fig. 5(f). Based on this hypothetical circuit, the feedback control loop for $\delta V_{\rm dc}$ can be devised, as shown in Fig. 6. The parts enclosed by the dashed lines in Fig. 6 denote the controller considered in this paper.

Based on the error between $\delta V_{\rm dc}$ and its reference, the PI controller modulates $i^*_{\rm np}$. Hereafter, the superscript "$*$" refers to the reference value. However, because $i_{\rm np}$ cannot be synthesized directly in the inverter, $i^*_{\rm np}$ should be converted to a type of variable that is implementable. As mentioned earlier, the zero-sequence voltage of $v_{\rm zs}$ can be exploited for this purpose. This conversion from $i^*_{\rm np}$ to $v^*_{\rm zs}$ is denoted as $z_{\rm np}$ in Fig. 6 and can be referred to as the neutral point impedance. Here, $z_{\rm np}$ is considered as like impedance, because the voltage $v^*_{\rm zs}$ is determined by the multiplication of the current, $i^*_{\rm np}$, and $z_{\rm np}$ in the block diagram. Although $v^*_{\rm zs}$ is the output of the controller, its practical effect on $\delta V_{\rm dc}$ appears through the neutral point current of $i_{\rm np}$ in the hypothetical equivalent circuit. This conversion from $v^*_{\rm zs}$ to $i_{\rm np}$ is denoted as $y_{\rm np}$, the neutral point admittance. The overall operation of $z_{\rm np}$ and $y_{\rm np}$ equates to the operation of an actuator.

The asymmetric limiter in Fig. 6 refers to the physical limitation of the inverter when attempting to synthesize $i_{\rm np}$. It is known that this limitation is dependent on operating conditions such as the power factor and modulation index [8], [9].

D. PI Gains for $\delta V_{\rm dc}$ Control

When (6) is assumed, (7) can be derived from Fig. 6. The assumption of (6-a) indicates a case in which the original reference of $i^*_{\rm np}$ is within the boundary of the limiter. In addition, (6-b) means that the actuator is ideal. Equation (6-c) implies that a sort of disturbance has been neglected when analyzing the closed-loop transfer function from $\delta V^*_{\rm dc}$ to $\delta V_{\rm dc}$

$$i^*_{\rm np} = i^*_{\rm np\_sat} \tag{6-a}$$

$$z_{\rm np}\cdot y_{\rm np} = 1 \tag{6-b}$$

$$i_{\rm np\_pv} = 0 \tag{6-c}$$

$$\left(\delta V^*_{\rm dc} - \delta V_{\rm dc}\right)\left(k_{\rm pn} + \frac{k_{\rm in}}{s}\right)\left(\frac{1}{sC_{\rm dc}} + R_{\rm dc}\right) = \delta V_{\rm dc} \tag{7}$$

where $k_{\rm pn}$ and $k_{\rm in}$ are the proportional and the integral gains.

When the PI gains in (9) satisfy (8), the transfer function from $\delta V^*_{\rm dc}$ to $\delta V_{\rm dc}$ is simplified into (10) from (7)

$$R_{\rm dc}k_{\rm pn} \approx 0, \quad k_{\rm pn}/k_{\rm in} \gg R_{\rm dc}C_{\rm dc} \tag{8}$$

$$k_{\rm pn} = 2\zeta\omega_n C_{\rm dc}, \quad k_{\rm in} = C_{\rm dc}\omega_n^2 \tag{9}$$

$$\frac{\delta V_{\rm dc}}{\delta V^*_{\rm dc}} \approx \frac{2\zeta\omega_n\cdot s + \omega_n^2}{s^2 + 2\zeta\omega_n\cdot s + \omega_n^2} \tag{10}$$

where ζ and ω_n are, respectively, the damping ratio and the bandwidth for the $\delta V_{\rm dc}$ control loop.

Because the transfer function takes the form of a low-pass filter (LPF), the parameter ω_n can be regarded as a type of bandwidth. This is useful to explicitly set the dynamic response of the closed loop regulating $\delta V_{\rm dc}$.

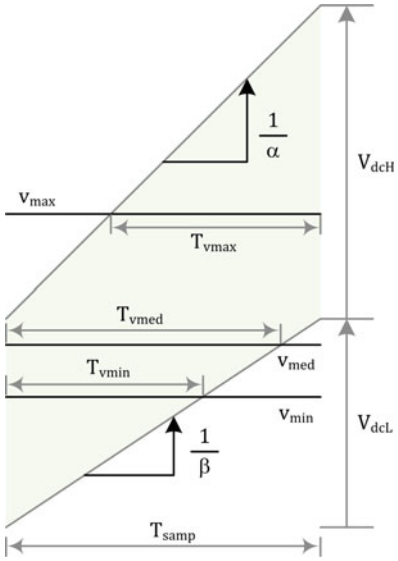

Fig. 7. Useful definitions to calculate average of neutral point current.

III. Analysis on Neutral Point Current

Although the feedback loops were closed for the asymmetric control of the split dc-link, some parts in the loop should be clarified for a better understanding. For simple analysis, it is assumed that the instantaneous sum of the output current of the inverter is always zero. In addition, the values of output currents and dc-link voltages were assumed to be constant during the sampling period.

A. Neutral Point Currents Depending on the Zero-Sequence Voltages

In order to regulate $\delta V_{\rm dc}$, it is important to adjust $i_{\rm np}$ precisely according to its reference. However, in the PWM inverter, $i_{\rm np}$ is indirectly synthesized through the switching operations. That is, the average value of $i_{\rm np}$ per sampling period, represented by $I_{\rm np}$, is the practical control target recognized by the digital signal processor (DSP). This average value can be computed through the other given states in the inverter. To derive the equation of $I_{\rm np}$, the following definitions were used. Namely, one of the voltage references is denoted by $v_{\rm max}$ if its value is maximal, by $v_{\rm med}$ if it is medial, and by $v_{\rm min}$ if it is minimal. In addition, as an example, the current whose phase corresponds to $v_{\rm max}$ is indicated by $i_{v\rm max}$. Then, $I_{\rm np}$ can be expressed as

$$I_{\rm np} = \frac{1}{T_{samp}}(T_{v\rm max}\cdot i_{v\rm max} + T_{v\rm med}\cdot i_{v\rm med} + T_{v\rm min}\cdot i_{v\rm min}) \tag{11}$$

where $T_{v\rm max}, T_{v\rm med}$, and $T_{v\rm min}$ are defined in Fig. 7: e.g., $T_{v\rm max}$ is the time when $v_{\rm max}$ is below the high-side carrier and simultaneously above the low-side carrier during a sampling period. Hereafter, this type of time is indicated as neutral connection time (NCT) because a phase terminal is connected to the neutral point only during the NCT. In addition, T_{samp} denotes a sampling period.

Adding a zero-sequence voltage of $v_{\rm zs}$ to voltage references leads to a parallel displacement of the references vertically, as shown in Fig. 7. Because this contributes to the variation of the NCT in each phase, $I_{\rm np}$ changes according to $v_{\rm zs}$. This is why the zero-sequence voltage is useful for the asymmetric control. Meanwhile, $I_{\rm np}$ directly depends on the output currents and the available range of each NCT changes according to the voltage references. Therefore, $I_{\rm np}$ can vary widely even with a fixed $v_{\rm zs}$ because the output currents and voltage references change at the fundamental frequency. That is, the conversion property of $y_{\rm np}$ depends on the operating conditions.

As depicted in Fig. 7, α and β, which are the slopes of the carriers, are defined, respectively, as

$$\alpha = T_{samp}/V_{\rm dcH} \text{ and } \beta = T_{samp}/V_{\rm dcL}. \tag{12}$$

With a positive increment of $v_{\rm zs}$, denoted as $\delta v_{\rm zs}$, the NCT changes according to $-\alpha\cdot\delta v_{\rm zs}$ if the reference intersects with the high-side carrier or according to $\beta\cdot\delta v_{\rm zs}$ if the reference intersects with the low-side carrier. That is, the variation of NCT due to $\delta v_{\rm zs}$ is reversed when the intersected carrier is changed.

When the modulation index is small enough, as in Fig. 7, all voltage references can intersect with only one carrier depending on $v_{\rm zs}$. This low modulation index was considered to include more diverse cases for the analysis of the $I_{\rm np} - v_{\rm zs}$ curve. The effects of $v_{\rm zs}$ were then taken into account piece-wise in the following intervals:

$$-V_{\rm dcL} - v_{\rm min0} \le v_{\rm zs} < -v_{\rm max0} \tag{13-a}$$

$$-v_{\rm max0} \le v_{\rm zs} < -v_{\rm med0} \tag{13-b}$$

$$-v_{\rm med0} \le v_{\rm zs} < -v_{\rm min0} \tag{13-c}$$

$$-v_{\rm min0} \le v_{\rm zs} < V_{\rm dcH} - v_{\rm max0} \tag{13-d}$$

where $v_{\rm max0}, v_{\rm med0}$, and $v_{\rm min0}$ are phase voltage references.

The smallest boundary value in (13-a) results in $v_{\rm min}$ being placed at the lowest boundary of the low-side carrier, while the largest boundary value in (13-d) leads to $v_{\rm max}$ being placed at the highest boundary of the high-side carrier. The rest of the boundary values in (13) can be determined such that one of the pole voltage references becomes zero by adding $v_{\rm zs}$ to the phase voltage references. The inflections in the $I_{\rm np} - v_{\rm zs}$ curve would be observed at these zero-crossing points.

When the value of $I_{\rm np}$ with the left boundary of $v_{\rm zs}$ in (13-a) is arbitrarily defined as $I_{{\rm np}\_a0}$, the variation of $I_{\rm np}$, denoted by $I_{\rm npA}(\delta v_{\rm zs})$, can be described via (14) within the interval. The argument of the function, $\delta v_{\rm zs}$, is an incremental amount of $v_{\rm zs}$ from the left boundary value

$$\begin{aligned} I_{\rm npA}(\delta v_{\rm zs}) &= I_{{\rm np}\_a0} + \frac{\delta v_{\rm zs}}{T_{samp}}(\beta i_{v\rm max} + \beta i_{v\rm med} + \beta i_{v\rm min}) \\ &= I_{{\rm np}\_a0} + \frac{\delta v_{\rm zs}\cdot\beta}{T_{samp}}(i_{v\rm max} + i_{v\rm med} + i_{v\rm min}) \\ &= I_{{\rm np}\_a0}. \end{aligned} \tag{14}$$

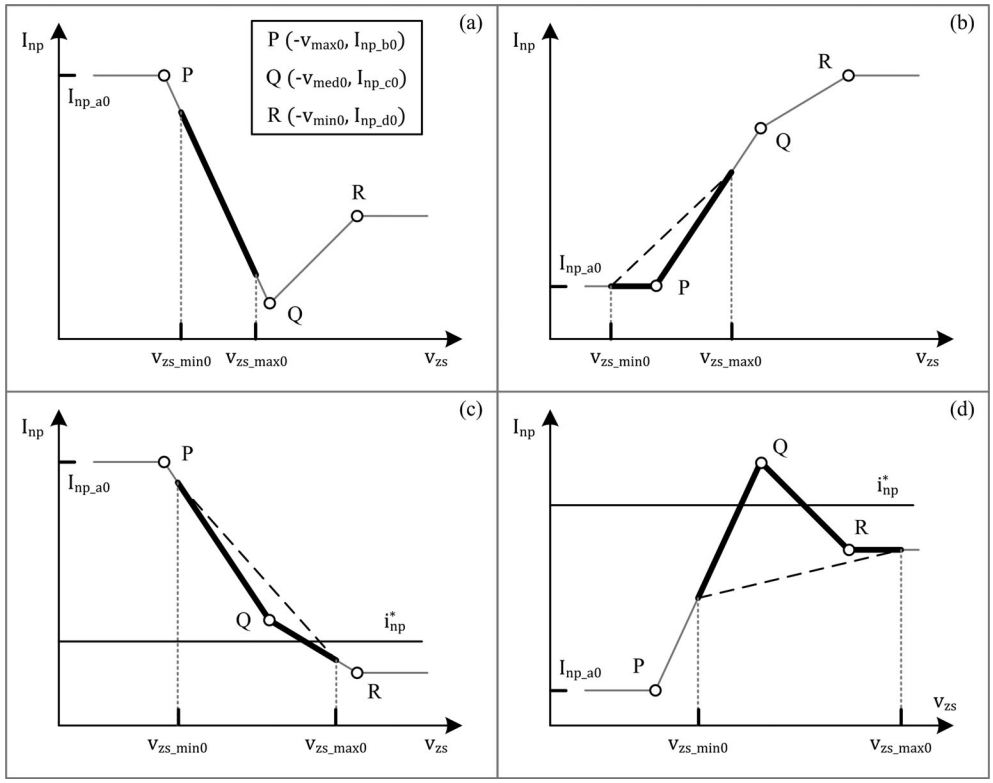

Fig. 8. $I_{\rm np} - v_{\rm zs}$ curves, (a) $i_{v\max} > 0, i_{v\min} > 0$, (b) $i_{v\max} < 0, i_{v\min} > 0$, (c) $i_{v\max} > 0, i_{v\min} < 0$, (d) $i_{v\max} < 0, i_{v\min} < 0$.

The variations of $I_{\rm np}$ in other intervals also can be derived as

$$\begin{aligned} I_{\rm npB}\left(\delta v_{\rm zs}\right) &= I_{\rm np\_b0} + \frac{\delta v_{\rm zs}}{T_{samp}}\left(-\alpha i_{v\max} + \beta i_{v\rm med} + \beta i_{v\min}\right) \\ &= I_{\rm np\_b0} + \frac{\delta v_{\rm zs}}{T_{samp}}\{\beta\left(i_{v\max} + i_{v\rm med} + i_{v\min}\right) \\ &\quad - (\alpha+\beta) i_{v\max}\} \\ &= I_{\rm np\_b0} - \frac{\delta v_{\rm zs}}{T_{samp}}(\alpha+\beta) i_{v\max} \qquad (15) \end{aligned}$$

$$I_{{\rm np}C}\left(\delta v_{\rm zs}\right) = I_{\rm np\_c0} + \frac{\delta v_{\rm zs}}{T_{samp}}(\alpha+\beta) i_{v\min} \qquad (16)$$

$$I_{{\rm np}D}\left(\delta v_{\rm zs}\right) = I_{\rm np\_d0}. \qquad (17)$$

Considering (14) to (17), it is noticeable that the $I_{\rm np} - v_{\rm zs}$ curve is piece-wise linear. Therefore, if one linear interval is selected properly, $z_{\rm np}$ and the asymmetric limiter in Fig. 6 can both be easily determined.

B. Effective Interval of Zero-Sequence Voltages for $z_{\rm np}$ and Asymmetric Limiter

Based on (13), (15), and (16), $I_{\rm np}$ can be altered by $v_{\rm zs}$ only within the interval given as

$$-v_{\max 0} \le v_{\rm zs} \le -v_{\min 0}. \qquad (18)$$

Therefore, it appears to be straightforward to find a useful linear interval by merely checking the inflection points on the $I_{\rm np} - v_{\rm zs}$ curve. However, the problem is that the available range of $v_{\rm zs}$ may not be identical to (18). That is, because the example of Fig. 7 was only a particular case whose modulation index is very low, the $I_{\rm np} - v_{\rm zs}$ curve under various modulation indexes should be taken into account comprehensively.

Because the values of $\delta v_{\rm zs}$, α, β, and $T_{\rm samp}$ were all positively defined, whether the slope of $I_{\rm np}$ per $\delta v_{\rm zs}$ is positive or negative depends on $i_{v\max}$ within (13-b) and on $i_{v\min}$ within (13-c) when considering (15) and (16). In addition, because the signs of $i_{v\max}$ and $i_{v\min}$ can be either positive or negative, varying aspects of the $I_{\rm np} - v_{\rm zs}$ curve can be generally categorized into the four cases shown in Fig. 8. Namely, the curves started from arbitrary values of $I_{{\rm np}\_a0}$ and were drawn based on (14) to (17) in each figure. The inflection points of P, Q, and R are indicated by their coordinates in Fig. 8(a). For convenience, the absolute values of $i_{v\max}$ are assumed to be larger than those of $i_{v\min}$. Even if this assumption does not hold, only the slope of each curve would change.

The $I_{\rm np} - v_{\rm zs}$ curve is shown in Fig. 8 as if all intervals in (13) are available. However, because the practical range of $v_{\rm zs}$ may be limited, this limitation was indicated by $v_{\rm zs\_min0} (= -V_{\rm dcL} - v_{\min 0})$ and $v_{\rm zs\_max0} (= V_{\rm dcH} - v_{\max 0})$. The practical $I_{\rm np} - v_{\rm zs}$ curves are highlighted with the bold lines as examples.

As shown in Fig. 6, the PI controller outputs $i^*_{\rm np}$. This reference can be depicted as a horizontal line as shown in Fig. 8(c) and (d). Then, if the $I_{\rm np} - v_{\rm zs}$ curve intersects with the reference line, $v_{\rm zs}$ at the intersection can be selected as the practical reference of $v^*_{\rm zs}$. The role of $z_{\rm np}$ in Fig. 6 is to obtain this corresponding $v_{\rm zs}$. Fortunately, because the $I_{\rm np} - v_{\rm zs}$ curve is piece-wise linear, $v^*_{\rm zs}$ can be computed simply by linear

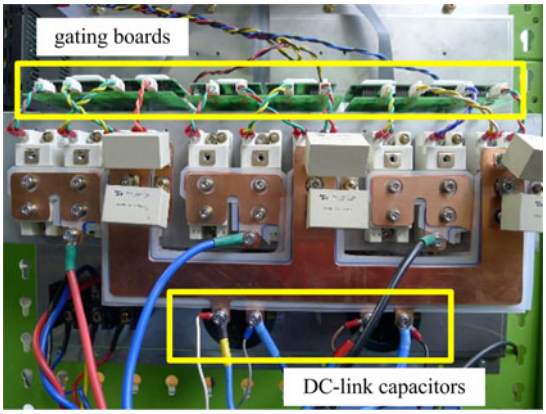

Fig. 9. Proto-type 5-kVA PV inverter.

interpolation if the boundary values of the intersected interval are identified. Even if the intersection does not occur, the identification of an effective interval is still useful to determine the limiting values of the asymmetric limiter in Fig. 6. Namely, one boundary value of the effective interval synthesizing the neutral point current closer to $i^*_{\rm np}$ can be selected as $v^*_{\rm zs}$.

IV. Experimental Result

A. Experimental Setups

To demonstrate the proposed control method, the PV inverter of 5 kVA shown in Fig. 9 was fabricated. Each capacitance of the split dc-link, $C_{\rm dc}$ in Fig. 5(f), was 3300 μF. Additionally, the inverter was connected to a line-to-line 140 $V_{\rm rms}$ 3ϕ grid via a three-phase *LCL* filter, whose inverter-side and grid-side inductances are 400 and 180 μH, respectively. The filter capacitors were delta-connected and their capacitances were 5.2 μF each. That is, the resonant frequency of the *LCL* filter was set at 3.6 kHz while the grid frequency was 60 Hz.

All control algorithms were implemented with a DSP board based on TMS320F28335. The carrier frequency was 7.5 kHz; the sampling frequency was 15 kHz. In addition, the dead time was set to 2.5 μs.

Under ideal conditions, the transfer functions for the *d–q* currents and $V_{\rm dc}$ are assumed to be

$$\frac{i}{i^*} = \frac{\omega_{\rm cc}}{s+\omega_{\rm cc}} \tag{19-a}$$

$$\frac{V_{\rm dc}}{V^*_{\rm dc}} = \frac{2\zeta_{\rm vc}\omega_{\rm vc}\cdot s+\omega^2_{\rm vc}}{s^2+2\zeta_{\rm vc}\omega_{\rm vc}\cdot s+\omega^2_{\rm vc}} \tag{19-b}$$

where $\omega_{\rm cc}$ is the bandwidth of the current control loop; $\zeta_{\rm vc}$ and $\omega_{\rm vc}$ are the damping ratio and the bandwidth of the $\rm V_{dc}$ control loop [19].

The bandwidth of the current control loop was set at $2\pi\cdot$200 rad/s, which means a rise time of 1.7 ms if the actuator has no limit. Because the bandwidth of the current control loop should be high enough compared to the bandwidth of the voltage control loop, which is the outer loop of the current control loop [19], the bandwidth for the $V_{\rm dc}$ control loop was set at $2\pi\cdot$10 rad/s with the unity damping ratio, which means a rise time of 12.5 ms. The gain settings of $V_{\rm dc}$ were identically applied to those of $\delta V_{\rm dc}$ in (10) because similar responses are expected for $V_{\rm dc}$ and $\delta V_{\rm dc}$, which are altered by the references from separate MPPTs.

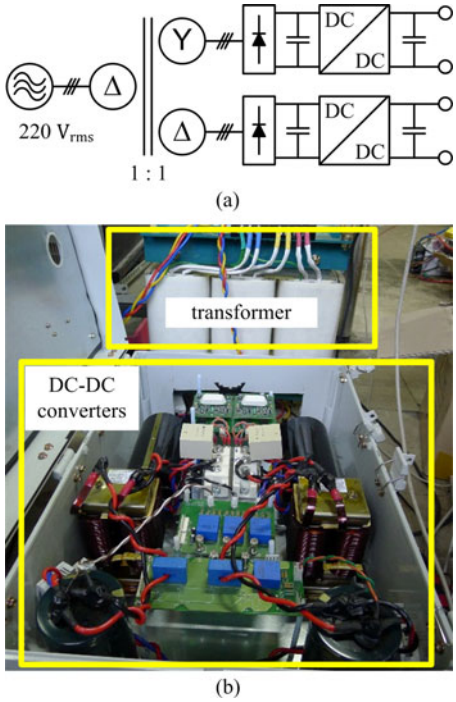

Fig. 10. PV simulator: (a) block diagram and (b) practical setup.

First, the $\delta V_{\rm dc}$ control was tested under a constant $V_{\rm dc}$. That is, terminals of a dc voltage source were connected to the nodes of "*p*" and "*n*" (see Fig. 1). The fundamental operations of the $\delta V_{\rm dc}$ control, newly proposed in this paper, could then be solely examined regardless of the $V_{\rm dc}$ control.

The PV simulator shown in Fig. 10 was designed to offer two isolated dc sources. As shown in Fig. 10(a), each output voltage can be separately adjusted by the dc–dc converters. For the experiments, these output ports were connected in series. That is to say, the negative terminal of the high-side port and the positive terminal of the low-side port were tied together. Three ports of the PV simulator were then connected to the dc-link of the inverter to simulate the system shown in Fig. 1. Using this setup, the regulations of $V_{\rm dc}$ and $\delta V_{\rm dc}$ were simultaneously tested.

B. Experimental Results Under a Constant $V_{\rm dc}$ Source

For independent tests of the $\delta V_{\rm dc}$ control, $V_{\rm dc}$ was set to 260 V. The average modulation index was 0.7627 when the grid currents were regulated at their rating of 29 $\rm A_{peak}$ with unity power factor.

The performance of the asymmetric control was confirmed when $\delta V^*_{\rm dc}$ was changed from -20 to 20 V. Practically, the slew rate of $\delta V^*_{\rm dc}$ was set to 150 V/s. Although higher slew rates were possible, this setting was sufficient when considering the entire MPPT range of 225 to 400 V. The gain settings in Section IV-A were enough to achieve a slew rate of 150 V/s. As shown in

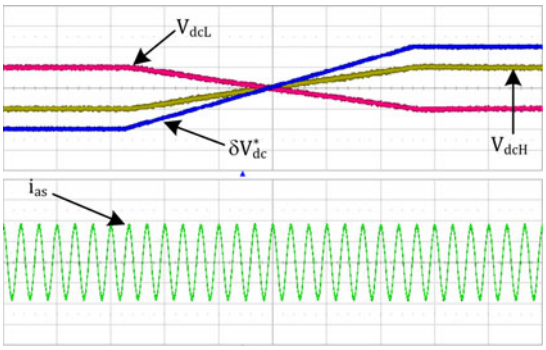

Fig. 11. Voltage variations under $\delta V_{\rm dc}$ control, $V_{\rm dcH}$ and $V_{\rm dcL}$ (10 V/div, center 130 V), $\delta V^*_{\rm dc}$ (10 V/div, center 0 V), i_{as} (4 A/div, center 0 A), Time (0.5 s/div).

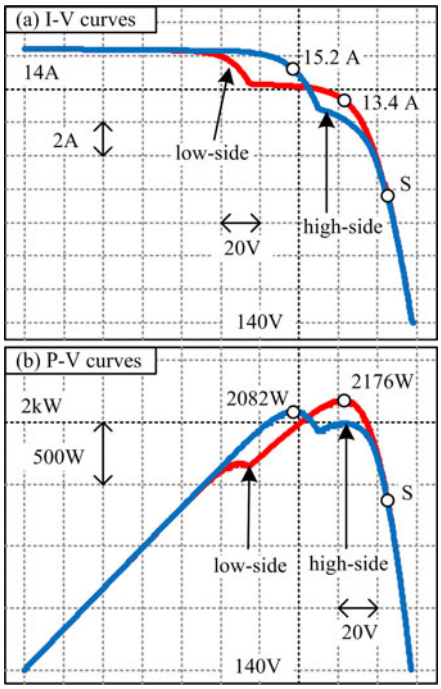

Fig. 12. Characteristic curves for the PV simulator: (a) current–voltage (*I–V*) curves and (b) power–voltage (*P–V*) curves.

Fig. 11, when the sum of $V_{\rm dcH}$ and $V_{\rm dcL}$ was maintained by the voltage source, each voltage was modulated according to its reference without causing any distortion in the grid current. In a practical system based on TMS320F28335, the execution time for the proposed control parts, including the PI controller, the asymmetric limiter and $z_{\rm np}$ in Fig. 6, was about 5 μs per sampling period.

C. Experimental Results With the PV Simulator

In order to consider a case in which $i^*_{\rm np\_sat}$ is not zero, the inverter was connected to a PV simulator. The operation of the PV simulator is based on the characteristic curves shown in Fig. 12. These curves were obtained from computer simulations on the PV module, where two strings are paralleled and each string consists of six series-connected cells. The physical parameters of the cell were quoted from earlier work [20]. In addition, it

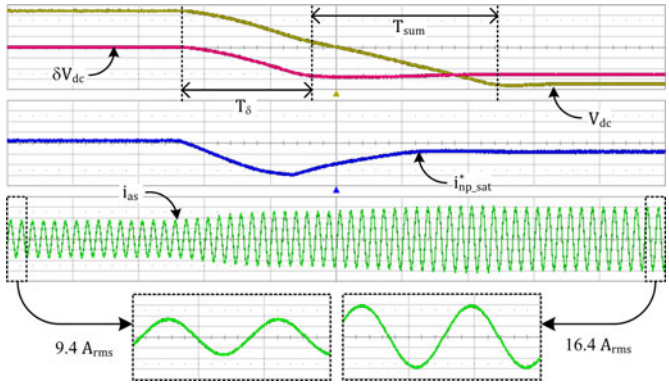

Fig. 13. Voltage regulations for maximum power generation, $V_{\rm dc}$(10 V/div, center 335 V), $\delta V_{\rm dc}$ (10 V/div, center 0 V), $i^*_{\rm np\_sat}$ (2.5 A/div, center 0 A), i_{as} (8 A/div, center 0 A), time (0.1 s/div, enlarged scale: 10 ms/div).

was assumed that the PV modules out of shade were under the standard test condition of 1000 W/m^2 and 25 °C. Partial shading was adjusted to obtain suitable characteristic curves. The reference to the output current of each dc–dc converter in Fig. 10 was then determined by the I–V curve in Fig. 12. For instance, the curve denoted by "high-side" was used for the converter whose output port is connected to the high-side capacitor of the inverter. According to the voltage of the high-side capacitor, the corresponding current in Fig. 12(a) was output as the current reference.

To examine the performance of the overall voltage controls, one simple scenario was planned, in which $V_{\rm dcH}$ and $V_{\rm dcL}$ were, respectively, changed from point S to the maximum power point in Fig. 12. This corresponds to the case in which $V^*_{\rm dc}$ changes from 370 to 300 V and $\delta V^*_{\rm dc}$ changes from 0 to -26 V. The experimental results are shown in Fig. 13.

Both slew rates of $V^*_{\rm dc}$ and $\delta V^*_{\rm dc}$ were set to 150 V/s. The variations of the actual values of $V_{\rm dc}$ and $\delta V_{\rm dc}$ were then nearly identical during the interval of T_δ in Fig. 13. When considering (1), these variations indicate that the voltage controls only served to reduce $V_{\rm dcH}$ during T_δ. As a result, $i^*_{\rm np\_sat}$ was rapidly decreased to counterbalance the current difference between the high-side and the low-side in Fig. 12(a).

After $\delta V_{\rm dc}$ converged to its reference, only $V_{\rm dc}$ was changed during $T_{\rm sum}$, indicating that both $V_{\rm dcH}$ and $V_{\rm dcL}$ started to decrease at the same ratio. As the voltages approached each maximum power point, $i^*_{\rm np\_sat}$ was converged to a final value of -1.8 A, as expected from Fig. 12(a).

As shown in Fig. 13, the grid current also increased from 9.4 to 16.4 $A_{\rm rms}$. Because the line-to-line voltage of the grid was 140 $V_{\rm rms}$, each current corresponds to 2.27 and 3.98 kW, respectively. At the maximum power point, the conversion efficiency of the inverter was 93.4%.

However, the advantage of the proposed control system was that two separate MPPTs on PV modules are possible by exploiting the intrinsically split dc-link of a single three-level inverter. Then, under the same conditions, the power generation of the proposed system should be compared to that of the conventional system, where the current path of $i_{\rm np\_pv}$ in Fig. 1 does not exist. The maximum power of the proposed system was 4258 W

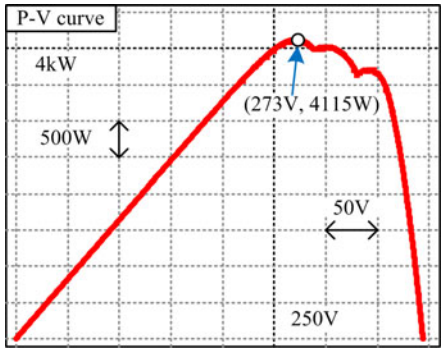

Fig. 14. *P–V* curve of the conventional system, where the neutral point of the PV modules is not connected to the three-level inverter.

overall, as shown in Fig. 12, whereas that of the conventional system was 4115 W as shown in Fig. 14. That is, by virtue of the proposed method, the available power can be increased by 3.5% even under the same PV module conditions.

V. Conclusion

The three-level inverter has some advantages as a grid-connected PV inverter because it has one more voltage level than the two-level inverter. In combination with this advantage, the proposed control method can contribute to the enhancement of the power generation from PV modules under given shading conditions, as separate MPPTs are possible in the proposed control system.

For the separate MPPTs, the dc-link voltages of the inverter have to be asymmetrically regulated. All of the blocks pertaining to this asymmetric regulation were described in this paper. In addition, the manner of setting the gains of the control loop was explicitly suggested.

The neutral point current in the three-level inverter is the important state for the asymmetric control. It can be indirectly controlled by the zero-sequence voltage. Thus, the correlation between them was mathematically analyzed. Based on this analysis, a method of appropriately selecting the zero-sequence voltages was explained in this paper. In particular, using a PV simulator, the proposed method could be tested even when asymmetric powers were transferred to each dc-link capacitor of the inverter. As an example, the proposed control system was examined when the total available power from the PV modules was increased by 3.5% under partial shading. This portion becomes more critical if the power rating of the PV generation system increases.

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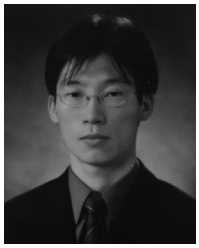

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