Analysis and Compensation of Inverter Nonlinearity for Three-Level T-Type Inverters

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***Abstract*—This paper analyzes the inverter nonlinearity effect resulting in issues such as narrow pulses and the even order harmonics in three-level T-type inverters. These issues make the compensation of the inverter nonlinearity be difficult. Based on the analysis of the output voltage distortion, carrier-based PWM methods to avoid these issues and to balance dc-link voltages simultaneously are proposed using the concept of the offset voltage. The proposed PWM methods can be easily implemented by adding appropriate offset voltages to output voltage references. Also, a compensation method to alleviate inverter nonlinearity effects is proposed based on the modeling of the inverter nonlinearity. The effectiveness of proposed methods is verified by experimental results. Through the proposed algorithms, not only even harmonics but also 5^{th} and 7^{th} harmonic components of current are conspicuously reduced. At the same time, the neutral voltage of the inverter can be balanced effectively by the proposed PWM methods.**

Keywords*—Inverter nonlinearity; three-level topology; T-type inverter; offset voltage; neutral point (NP) voltage control

I. INTRODUCTION

Multi-level Pulse-Width Modulation (PWM) Voltage Source Inverters (VSIs) are getting attentions thanks to their advantages over two-level VSIs such as better harmonic characteristics, smaller *dv/dt*, and higher efficiency. Among many multi-level inverters, three-level inverters such as Neutral Point Clamped (NPC) topology and T-type topology have been widely used because of their relatively simple control and technical maturity. Compared to NPC topology, T-type topology is more preferred particularly in low voltage applications where the conduction losses could be minimized due to the reduced number of switching semiconductors [1].

However, due to increased number of switching states, the effect of the inverter nonlinearity in three-level topology is more complicated compared to that in two-level topology. Inverter nonlinearities coming from the dead time, parasitic capacitors, and voltage drop across switching devices provoke the distortion of the output voltage of the inverter and degrades overall performances of the variable speed electric machine drive system.

There have been many researches on the inverter nonlinearity compensation for two-level inverter [2]-[9]. In the early literatures [2]-[5], inverter nonlinearity effects had been compensated by adding a compensation voltage to voltage references [2]-[3] or adjusting the length of gating pulses [4]-[5]. The effect of parasitic capacitances [5]-[7] and voltage drop across switching devices [2], [7] had been included to improve the compensation accuracy. Also, the inverter nonlinearity in multi-level inverters and its compensation have been addressed in several papers [10]-[12]. However, the analysis of inverter nonlinearity effects was done similarly to that of two-level inverter. And, the most of previous works have not considered the special characteristics of three-level T-type inverters.

The majority of them didn't cover output voltage distortion induced by, so called, narrow pulse problem [8]-[9] that occurs when pole voltage references are near the edges of PWM carriers. Since this problem becomes more severe in the case of multi-level inverters, it should definitely be considered and compensated. In [12], the narrow pulse problem in over-modulation region was considered on the basis of Space Vector PWM (SVPWM). Nevertheless, SVPWM method was complicated to accommodate the compensation algorithm against the narrow pulse problem because the on-time of each switch of the inverter should be geometrically computed. Compared to SVPWM method, the carrier-based PWM method has been known to be equivalent to SVPWM but simple to implement and could avoid narrow pulse problem instinctively. Also, even order harmonics from the nonlinearity of T-type inverters have not been covered properly, although it causes considerable distortion of the output voltage.

In this paper, inverter nonlinearity effects of three-level T-type inverter resulting in the narrow pulse and even order harmonic issues are addressed in detail. Based on the analyses, a carrier-based PWM technique and a compensation method to alleviate inverter nonlinearity effects are proposed. In proposed PWM methods, not only output voltage linearity but also controllability of Neutral Point (NP) voltage are considered. By adjusting essential parameters in the proposed PWM methods,

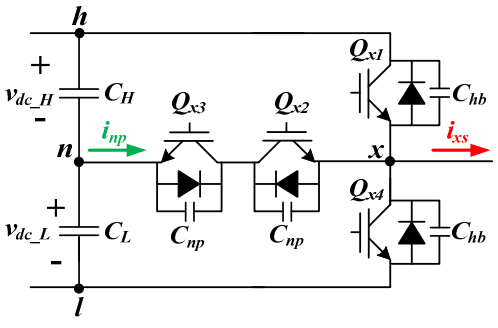


Fig. 1. One leg of a T-type inverter.

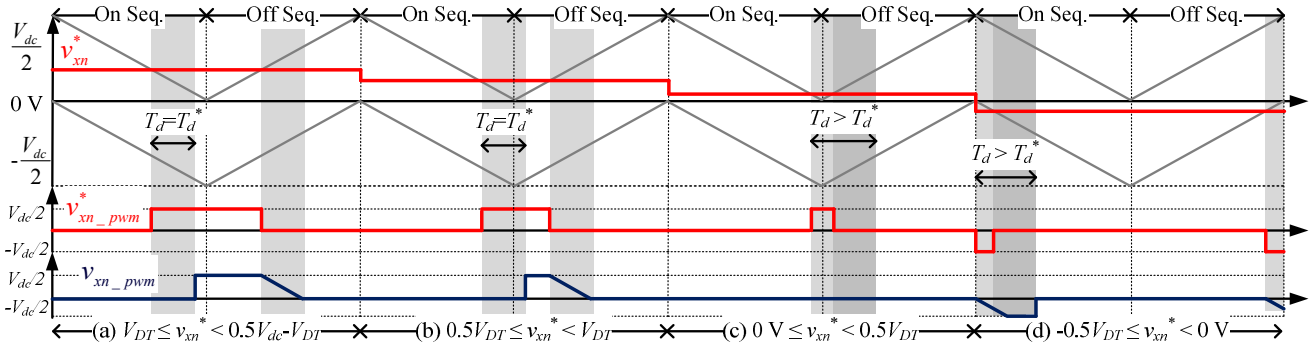


Fig 2. Dead time effect due to narrow pulses.

NP balancing could be realized at the same time. Several experimental results are provided to verify the validity of the proposed method.

II. Analysis of Inverter Nonlinearity Effects in Three-Level T-Type Inverters

Fig. 1 shows one leg of a T-type inverter, where x denotes an arbitrary phase among a, b, and c. Because of the junction capacitance of the semiconductor switches, there are naturally parasitic capacitors connected in parallel with the half-bridge switches (C_{hb}) and bidirectional switches (C_{np}). For the output pole voltage, v_{xn}, three switching states can be defined as follows: "H" state when phase current, i_{xs}, flows through the upper switch, "M" state, through the bidirectional switch, and "L" state, through the lower switch.

There are two main effects that provoke output voltage error, δv_{xn}, defined as (1), where v_{xn}^* indicates a pole voltage reference, and v_{xn}, actual pole voltage. Note that all the variables in (1) are per-switching-cycle average quantities.

$$\delta v_{xn} = v_{xn}^* - v_{xn} \ . \tag{1}$$

A. Dead time effect due to narrow pulses

At first, the voltage distortion from the narrow pulse can be depicted as Fig. 2, where the dead time is set as T_d. Fig. 2 shows generation of x-phase pole voltage in a three-level inverter based on level-shifted carrier waves, considering the dead time effect. In this figure, the values with subscript 'pwm' indicate instantaneous quantities and V_{DT} is defined as $V_{DT} = T_d / T_{sw} \cdot V_{dc}$. If v_{xn}^* is between V_{DT} and $(0.5V_{dc}-V_{DT})$ as shown in Fig. 2(a), the dead time effect in three-level inverters is very similar with that in two-level inverters. At on-sequence, where the switches are turning on, the output voltage is simply delayed by T_d, which leads to volt-sec loss in the inverter output. At off-sequence, where the switches are turning off, the output voltage doesn't fall instantly after the gating signal is turned off because of the parasitic capacitors, which leads to volt-sec gain in the inverter output. In this condition, the falling rate is determined by the parasitic capacitances and the current during the dead time. When v_{xn}^* is set between $0.5V_{DT}$ and V_{DT} as shown in Fig. 2(b), the dead time at on-sequence affects the output voltage at off-sequence. However, the dead time effect in this case is the same as that in the previous case for a switching-period in the average manner. However, if v_{xn}^* is close to 0V as shown in Fig. 2(c), the actual pole voltage v_{xn_pwm} is clamped to 0V because the two dead time durations at on and off sequences are overlapped and then turn-on signal for the switch is cut off. This phenomenon is called narrow pulse problem [8]. If v_{xn}^* is negative and is getting closer to the peak of the carrier, larger distortion occurs in the output voltage as shown in Fig. 2(d).

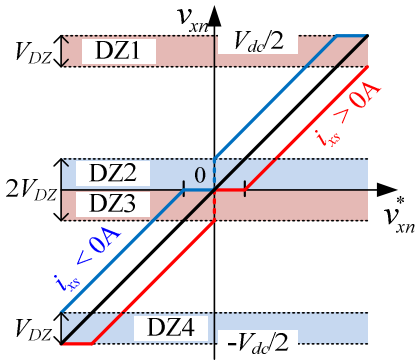


Fig. 3. Relation between v_{xn}^* and i_{xs} disregarding parasitic capacitors.

Fig. 3 shows the distortion of the output voltage assuming that the parasitic capacitor doesn't exist. In this figure, $V_{DZ}=0.5V_{DT}$ and four regions, denoted as DZ1-DZ4 whose widths are determined by V_{DZ}, indicate dead zones where the output voltage can't be synthesized properly. DZ1 and DZ3 arise with the positive phase current, whereas DZ2 and DZ4 arise with the negative phase current. This narrow pulse problem has already been investigated for two-level inverters [8]-[9]. However, this problem occurs in two-level inverters only under high Modulation Index (MI) operation where v_{xn}^* goes near the peak or valley of the carrier wave, e.g. in the case near or at over-modulation range. However, in three-level inverters, such problem could occur even under low MI operation since DZ2 and DZ3 are located at near zero voltage, which hasn't been sufficiently covered in the previous literatures.

Considering all the above-mentioned behaviors, the voltage error induced by the dead time, δv_{xn_DT}, can be derived from the difference between $v_{xn\_pwm}^*$ and v_{xn_pwm} within a switching period. δv_{xn_DT} at outside of the dead zones can be expressed as (2), where C_{eff} is effective parasitic capacitance which is defined as (3). Note that δv_{xn_DT} in (2) is an averaged value in a switching period. δv_{xn_DT} according to i_{xs} and v_{xn}^* with f_{sw}=10 kHz, T_d=3 μs, and V_{dc}=310 V is illustrated in Fig. 4. It is worth noting that δv_{xn_DT} is not only a function of the current but also affected by the voltage reference itself.

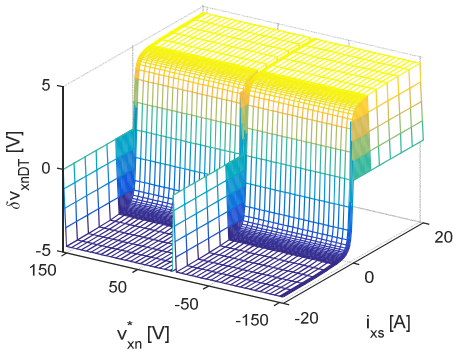


Fig. 4. δv_{xn_DT} according to i_{xs} and v_{xn}^*.

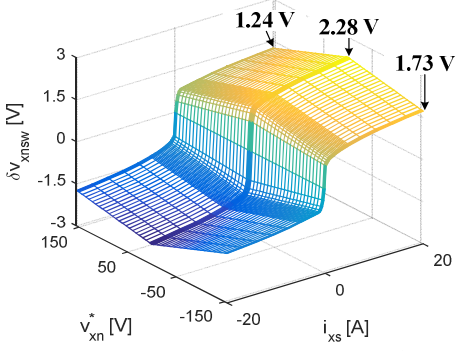


Fig. 5. δv_{xn_SW} according to i_{xs} and v_{xn}^*.

$$\delta v_{xn\_DT} = \begin{cases} -\frac{1}{8}\frac{C_{eff}V_{dc}^2}{T_{sw}}\frac{1}{i_{xs}} - \frac{T_d}{T_{sw}}\frac{V_{dc}}{2}. & (i_{xs} \le -I_{crit}) \\ \frac{T_d}{T_{sw}}\frac{T_d}{2C_{eff}}i_{xs}. & (-I_{crit} \le i_{xs} < I_{crit}) \\ -\frac{1}{8}\frac{C_{eff}V_{dc}^2}{T_{sw}}\frac{1}{i_{xs}} + \frac{T_d}{T_{sw}}\frac{V_{dc}}{2}. & (I_{crit} \le i_{xs}) \end{cases} \quad (2)$$

$$C_{eff} = 2C_{hb} + C_{np}. \quad (3)$$

B. Voltage drop of switching devices

In T-type inverters, pole voltage error induced by voltage drop of switching devices, δv_{xn_SW}, depends on the switching state. As shown in Fig. 1, the current should flow through the two switches, Q_{x2} and Q_{x3}, for "M" state, while, only one switch is in the current conduction path at "H" and "L" states. For this reason, δv_{xn_SW} at "M" state is distinctively large compared with that at other states. Considering the duty ratio, per-switching-cycle average value of δv_{xn_SW} can be modeled as a function of i_{xs} and v_{xn}^*. Fig. 5 shows δv_{xn_SW} according to i_{xs} and v_{xn}^* in the case of 1200V, 80A T-type IGBT module (VINCOTECH 10-FZ12NMA080SH01-M260F), which is used in the experiments. In this figure, it can be seen that the voltage error becomes larger as the magnitude of v_{xn}^* is getting smaller. The reason is that the duty ratio of the bidirectional switch increases as the magnitude of v_{xn}^* is getting reduced to zero.

Total voltage error is simply a sum of δv_{xn_DT} and δv_{xn_SW}, i.e., $\delta v_{xn} = \delta v_{xn\_DT} + \delta v_{xn\_SW}$. Because δv_{xn_SW} takes large portion in δv_{xn} compared to the case of two-level inverters, the dependency of δv_{xn_SW} on v_{xn}^* should be considered carefully.

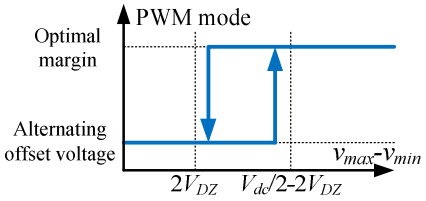


Fig. 6. Transition of PWM mode.

III. Proposed Scheme

As described in Fig. 3-4, it is physically impossible to synthesize v_{xn} in the dead zones. For proper synthesis of the output voltage, pole voltage references, $\mathbf{v}_{\mathbf{abcn}}^* \equiv \begin{bmatrix} v_{an}^* & v_{bn}^* & v_{cn}^* \end{bmatrix}^T$, should be located outside of region where the dead time effect is dominant, so called as the dead zones. In the carrier-based PWM method, this can be implemented by adding an offset voltage which is also called zero sequence voltage, v_{sn}^*, to phase voltage references, $\mathbf{v}_{\mathbf{abcs}}^* \equiv \begin{bmatrix} v_{as}^* & v_{bs}^* & v_{cs}^* \end{bmatrix}^T$. This operation is expressed as (4).

$$v_{xn}^* = v_{xs}^* + v_{sn}^*. \quad (4)$$

In the proposed scheme, PWM method to avoid the dead zones is changed according to v_{max}-v_{min} as shown in Fig. 6, where v_{max} and v_{min} are defined as (5). For stable transition, hysteresis is applied in the transition function. Under the assumption that $\mathbf{v}_{\mathbf{abcn}}^*$ are properly located off the dead zones, the inverter nonlinearity can be compensated using a compensation function according to i_{xs} and v_{xn}^*.

$$\begin{aligned} v_{\max} &= \max(\mathbf{v}_{\mathbf{abcs}}^*). \\ v_{\min} &= \min(\mathbf{v}_{\mathbf{abcs}}^*). \end{aligned} \quad (5)$$

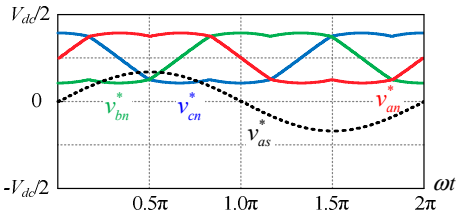
A. Technique to avoid dead zone using alternating offset voltage PWM

When $\mathbf{v}_{\mathbf{abcs}}^*$ are small in low MI operation, shifting all of $\mathbf{v}_{\mathbf{abcs}}^*$ to the middle of a carrier is the only way to avoid the dead zones. By doing so, the output voltage can be generated by only two switching states, "H" and "M" states or "M" and "L" states. By excluding one switching state, three-level inverters can operate like two-level inverter in low MI operation. One of the most popular settings of the offset voltage for two-level VSIs can be expressed as (6), which is known as equivalent to three-phase symmetry SVPWM [13]. This method will be called as Symmetrical Continuous PWM (SCPWM) hereafter. Since $\mathbf{v}_{\mathbf{abcn}}^*$ generated by (6) cross the dead zones when using three-level inverters, it can be modified to positive offset voltage, (7), or negative offset voltage, (8), which also minimizes sideband harmonics at the carrier frequency. Fig. 7(a) shows the waveform of $\mathbf{v}_{\mathbf{abcn}}^*$ using (7).

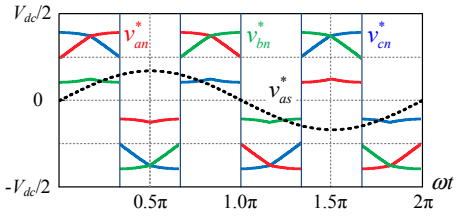
$$v_{sn}^* = -\frac{v_{\max} + v_{\min}}{2}. \quad (6)$$

$$v_{sn}^* = -\frac{v_{\max} + v_{\min}}{2} + \frac{v_{dc\_H}}{2}. \quad (7)$$

$$v_{sn}^* = -\frac{v_{\max} + v_{\min}}{2} - \frac{v_{dc\_L}}{2}. \quad (8)$$

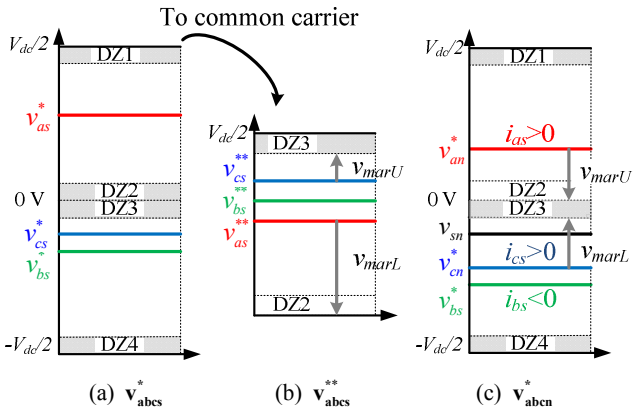


(a) $\mathbf{v}^*_{\mathbf{abcn}}$ using (7)



(b) $\mathbf{v}^*_{\mathbf{abcn}}$ using alternating offset voltage

Fig. 7. Waveform of $\mathbf{v}^*_{\mathbf{abcn}}$ at low MI.



(a) $\mathbf{v}^*_{\mathbf{abcs}}$ (b) $\mathbf{v}^{**}_{\mathbf{abcs}}$ (c) $\mathbf{v}^*_{\mathbf{abcn}}$

Fig. 8. Principle of optimal margin PWM.

However, applying either (7) or (8) provokes even order harmonics in the output voltage. Even order harmonics come up due to the asymmetry of δv_{xn_SW} shown in Fig. 5. Since δv_{xn_SW} becomes larger as v_{xn}^* is closer to zero, v_{xn}^* in Fig. 7(a) suffers more voltage loss at valley than at peak, which breaks half-wave symmetry of the output voltage, i.e., $\delta v_{xn}(\theta) \neq -\delta v_{xn}(\theta\text{-}180°)$. To satisfy $\delta v_{xn}(\theta) = -\delta v_{xn}(\theta\text{-}180°)$, v_{sn}^* can be changed between (7) and (8) alternately with 120° period as depicted in Fig. 7(b). Using this method, namely Alternating Offset Voltage PWM (AOVPWM), even order harmonics in the output voltage can be successfully diminished.

B. Technique to aviod dead zone using optimal margin PWM

Over a certain MI, $\mathbf{v}^*_{\mathbf{abcn}}$ can reach the dead zones even though AOVPWM is applied. In this case, one or two of $\mathbf{v}^*_{\mathbf{abcn}}$ have to be located in upper carrier region and the other has to be located in lower carrier region. In the region with middle and high MI, the optimal margin PWM (OMPWM) method can be used to avoid the dead zones.

As a basic principle, OMPWM optimizes the voltage margin between $\mathbf{v}^*_{\mathbf{abcn}}$ and the dead zones which can be utilized for balancing the upper and lower capacitor voltages of dc-link

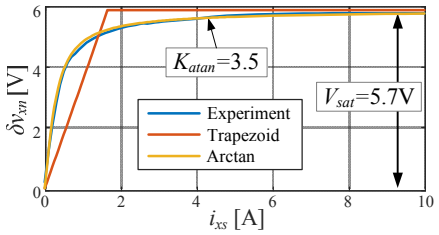


Fig. 9. δv_{xn} and v_{xn_Comp1}.

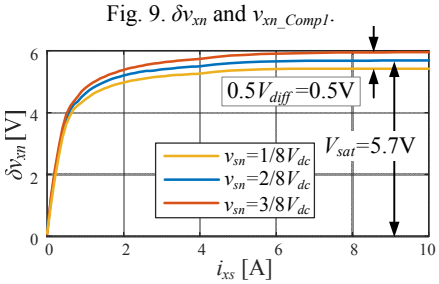


Fig. 10. Experimentally measured δv_{xn} according to v_{sn}.

of the three-level inverters. Fig. 8 shows the setting $\mathbf{v}^*_{\mathbf{abcn}}$ in OMPWM method. If $\mathbf{v}^*_{\mathbf{abcs}}$ is given as in Fig. 8(a), negative phase voltages are shifted to the upper carrier region by applying (9) as seen in Fig. 8(b). In the figure, v_{marU} and v_{marL} indicate upper and lower voltage margin, respectively. The dead zones are affected by the polarity of the current. For example, if $i_{as} > 0$ and $i_{cs} > 0$ in Fig. 8(b), DZ3 is effective but DZ2 isn't. In this case, v_{marU} and v_{marL} can be computed by (10). In order to avoid the dead zones and to secure maximum voltage margin, it is appropriate to set $|v_{marU}|=|v_{marL}|$. For maximum voltage margin, the offset voltage can be set as (11). Fig. 8(c) shows $\mathbf{v}^*_{\mathbf{abcn}}$ after applying (11). It can be found that the magnitudes of v_{marU} and v_{marL} become the same in the figure.

$$v_{xs}^{**} = v_{xs}^{*} + V_{dc}/2 \ . \tag{9}$$

$$\begin{aligned} v_{marU} &= V_{dc}/2 - V_{DZ} - v_{cs}^{**} . \\ v_{marL} &= 0\,\mathrm{V} - v_{as}^{**} . \end{aligned} \tag{10}$$

$$v_{sn}^{*} = \frac{v_{marU} + v_{marL}}{2} \ . \tag{11}$$

C. Compensation of inverter nonlinearity

Fig. 9 shows experimentally measured δv_{xn} according to i_{xs}, with v_{sn} set as (7) to locate the $\mathbf{v}^*_{\mathbf{abcn}}$ off the dead zones. The performance of the inverter nonlinearity compensation is determined by the shape of compensation function, v_{xn_Comp}. Among many compensation functions such as a step function, a trapezoidal voltage, and an arctangent function, the arctangent function defined as (12) is selected for the compensation function since it exhibits great agreement with the actual δv_{xn} as shown in Fig. 9. v_{xn_Comp1} is suitable for conventional NPC topology because the difference of δv_{xn_SW} between switching states would be negligible.

$$v_{xn\_Comp1} = V_{sat} \cdot \frac{2}{\pi} \arctan(K_{\mathrm{atan}} \cdot i_{xs}) \ . \tag{12}$$

In T-type inverter, δv_{xn_SW} is not only a function of the current but also affected by pole voltage reference. To consider asymmetric δv_{xn_SW}, the compensation function should be modified like v_{xn_Comp2} as shown in (13), where V_{diff} means the difference of δv_{xn} between "M" state and "H" or "L" state. To get V_{diff} experimentally, δv_{xn} should be extracted in various v_{sn} at outside of the dead zones. Fig. 10 shows experimentally measured δv_{xn} according to v_{sn}. The resistance of switch modules is excluded when δv_{xn} is extracted because it cannot be distinguished from that of load connected to the inverter.

$$v_{xn\_Comp2} = (V_{sat} + V_{diff}(\frac{|v_{xn}^*|}{0.5V_{dc}} - 0.5)) \cdot \frac{2}{\pi}\arctan(K_{a\tan} \cdot i_{xs}) . \quad (13)$$

IV. Voltage Balancing Control of Proposed Scheme

For three-level inverters, NP current causes the voltage difference between capacitors in the dc-link. NP balancing algorithms are widely discussed in the past literatures [14]-[16]. But none of them have dealt with the compensation of inverter nonlinearity effects because the offset voltage selection was only based on NP balancing objective. v_{xn}^* determined by conventional NP balancing algorithms could be located in the dead zones. Hence, NP balancing control should consider inverter nonlinearity effects to minimize the distortion of the output voltage.

Conventional NP balancing methods aren't compatible with the proposed PWM methods because both algorithms use the offset voltage simultaneously for different purposes. This problem is not severe for three-level converters with active front-ends such as boost PWM converter where either the offset voltage of PWM converter or that of PWM inverter could be used to balance NP potential. However, considering passive front ends such as diode rectifier, voltage balancing controls incorporated with the proposed PWM methods should be devised for maintaining voltage balance at NP. Proposed NP controllers in this paper are optimized for each PWM method. It has a low impact on original PWM algorithms at slight dc-link unbalance conditions and is easy to implement. And, it reveals better THD performance than other NP balancing algorithms.

A. Analysis of NP current versus offset voltage

NP current averaged over a switching period, i_{np} shown in Fig. 1, can be analytically calculated [14]-[15]. Measured dc-link voltages, v_{dc_H} and v_{dc_L} defined in Fig. 1, are used to synthesize proper v_{xn}^* even when the difference between high- and low-side dc-link voltages, $\delta v_{dc} \equiv v_{dc\_H} - v_{dc\_L}$, exists. i_{np} can be calculated in three-phase system as (14), where D_{xn} is duty ratio to neutral point which is defined as (15).

$$i_{np} = D_{an}i_a + D_{bn}i_b + D_{cn}i_c . \quad (14)$$

$$D_{xn} = \begin{cases} 1 + v_{xn} / v_{dc\_L} & (v_{xn} < 0) \\ 1 - v_{xn} / v_{dc\_H} & (v_{xn} \geq 0) \end{cases} . \quad (15)$$

i_{np} varies according to v_{sn}, so adding a proper offset voltage is a key factor to minimize δv_{dc}. The relationship between i_{np} and v_{sn} can be derived as (16), where v_{max}, v_{mid}, and v_{min} are defined as the maximum, medium, and minimum pole voltages, respectively. i_{max}, i_{mid}, and i_{min} are the currents of corresponding

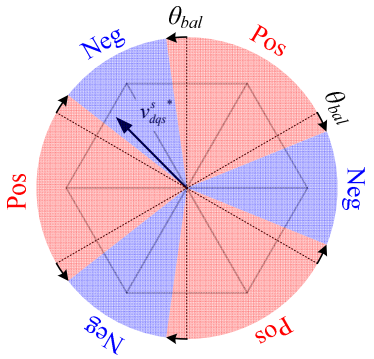


Fig. 11. Principle of NP balancing for AOVPWM.

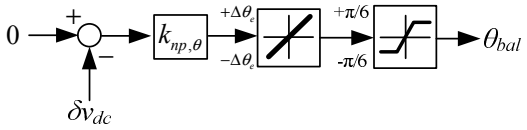


Fig. 12. Block diagram of NP controller for AOVPWM.

phases. To simplify the analysis, the output power, P_{out} defined as (17), is assumed to be a constant over an electrical rotating period.

$$i_{np} = \begin{cases} -\frac{P_{out}}{v_{dc\_H}} & (v_{sn} \geq -v_{\min}) \\ -\frac{P_{out}}{v_{dc\_H}} + (\frac{1}{v_{dc\_H}} + \frac{1}{v_{dc\_L}})(v_{\min} + v_{sn})i_{\min} & (-v_{\mathrm{mid}} \leq v_{sn} < -v_{\min}) \\ \frac{P_{out}}{v_{dc\_L}} - (\frac{1}{v_{dc\_H}} + \frac{1}{v_{dc\_L}})(v_{\max} + v_{sn})i_{\max} & (-v_{\max} \leq v_{sn} < -v_{\mathrm{mid}}) \\ \frac{P_{out}}{v_{dc\_L}} & (v_{sn} < -v_{\max}) \end{cases} . \quad (16)$$

$$P_{out} = v_{\max}i_{\max} + v_{mid}i_{mid} + v_{\min}i_{\min} . \quad (17)$$

B. NP controller for alternating offset voltage PWM

All pole voltages are shifted to one of the carrier region for AOVPWM. And, when the positive offset voltage, (7), is applied, all pole voltages are positive, i.e., $v_{sn} \geq -v_{min}$. But when the negative offset voltage, (8), is applied, all pole voltages are negative, i.e., $v_{sn} < -v_{max}$. In either condition, i_{np} can't be changed by shifting v_{sn}. But, the polarity of i_{np} is different in the case of (7) and (8). And, NP balancing can be achieved by controlling the ratio of each offset voltage.

Fig. 11 shows the principle of NP balancing for AOVPWM. NP current averaged over an electrical rotating period, $\bar{i}_{np}$, can be adjusted by balancing angle, θ_{bal}. $\bar{i}_{np}$ can be expressed as a linear function of θ_{bal} in (18).

$$\begin{aligned} \bar{i}_{np} &= \frac{1}{2\pi}\int_0^{2\pi} i_{np}(\theta)d\theta \\ &= \frac{P_{out}}{2}(\frac{1}{v_{dc\_L}} - \frac{1}{v_{dc\_H}}) - \frac{3P_{out}}{\pi}(\frac{1}{v_{dc\_L}} + \frac{1}{v_{dc\_H}})\theta_{bal} \end{aligned} . \quad (18)$$

NP controller for AOVPWM, namely θ_{bal} controller, consists of proportional gain, rate limiter, and limiter as shown

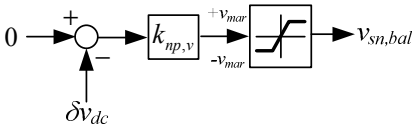


Fig. 13. Block diagram of NP controller for OMPWM.

in Fig. 12. The rate limiter is chosen to suppress rapid variation of offset voltage in low rotating speed. When NP controller is operated continuously, δv_{dc} would converge to zero voltage, i.e. $v_{dc\_H}=v_{dc\_L}$. Then, the relation between $\bar{i}_{np}$ and θ_{bal} can be simplified and the gain of controller, $k_{np,\theta}$, can be set as (19), where ω_{vc} is the bandwidth of NP control loop.

$$k_{np,\theta} = -\frac{\pi}{12} C_{dc} V_{dc} \frac{\omega_{vc}}{P_{out}}. \tag{19}$$

C. NP controller for optimal margin PWM

Under OMPWM, there can be only on or two positive pole voltages since v_{sn} is limited as $-v_{\max} \le v_{sn} < -v_{\min}$. In this v_{sn} range, i_{np} can be changed by shifting v_{sn}. Fig. 13 shows the block diagram of NP controller for OMPWM. Balancing offset voltage, $v_{sn,bal}$, is determined by proportional controller with limiter. It has similar structure with the dc common-mode voltage injection algorithm [16]. But the limiter is added to constraint $v_{sn,bal}$ within v_{mar} to keep pole voltage references out of the dead zones. The proportional gain, $k_{np,v}$, can be set in consideration of the performance of NP balancing and current harmonics. It can be set as -0.5 because it locates pole voltage references center of dc-link voltage. Proposed NP controllers can be utilized not only for motoring but also regenerative operation by changing sign of output variables, θ_{bal} or $v_{sn,bal}$.

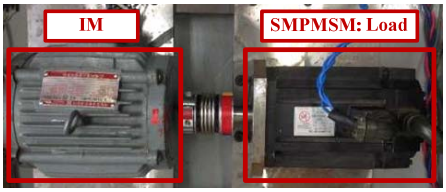


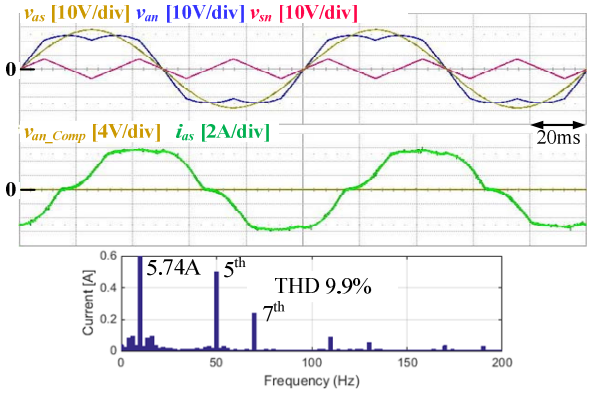
Fig. 14. Experimental Setup.

TABLE I. PARAMETERS OF INDUCTION MOTOR

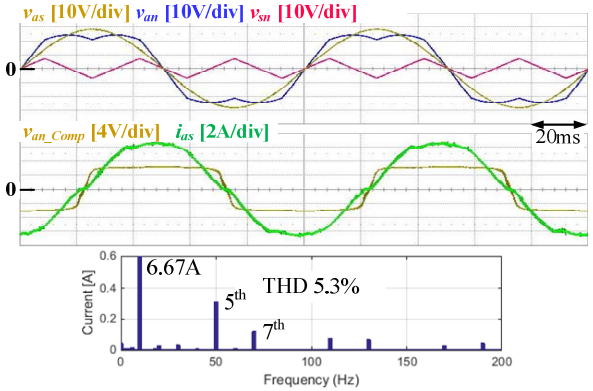
Parameter	Value
Rated Power	3.7 kW
Pole number	4
R_s / R_r	0.22 Ω / 0.3 Ω
L_m	63.62 mH
L_{ls} / L_{lr}	2.44 mH / 2.44 mH
Rated torque	11.5 N·m

V. EXPERIMENTAL RESULTS

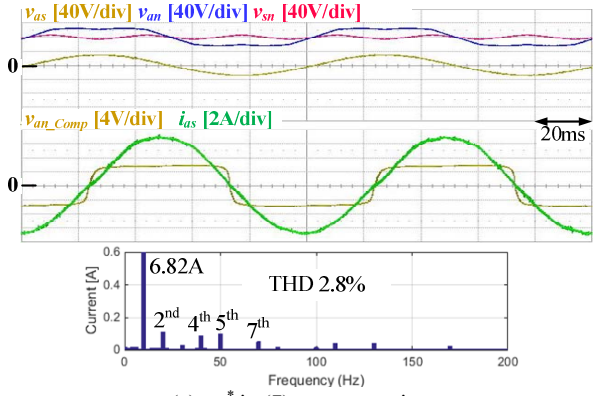
The experimental setup for the verification of the proposed scheme has been built as shown in Fig. 14. The induction machine under test is controlled by a three-level T-type inverter. The parameters of the induction machine are shown in Table I. The target machine is simply driven by V/f control.



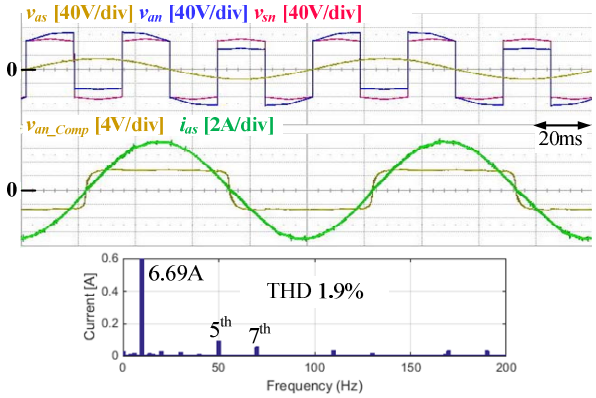
(a) SCPWM, no compensation



(b) SCPWM, compensation

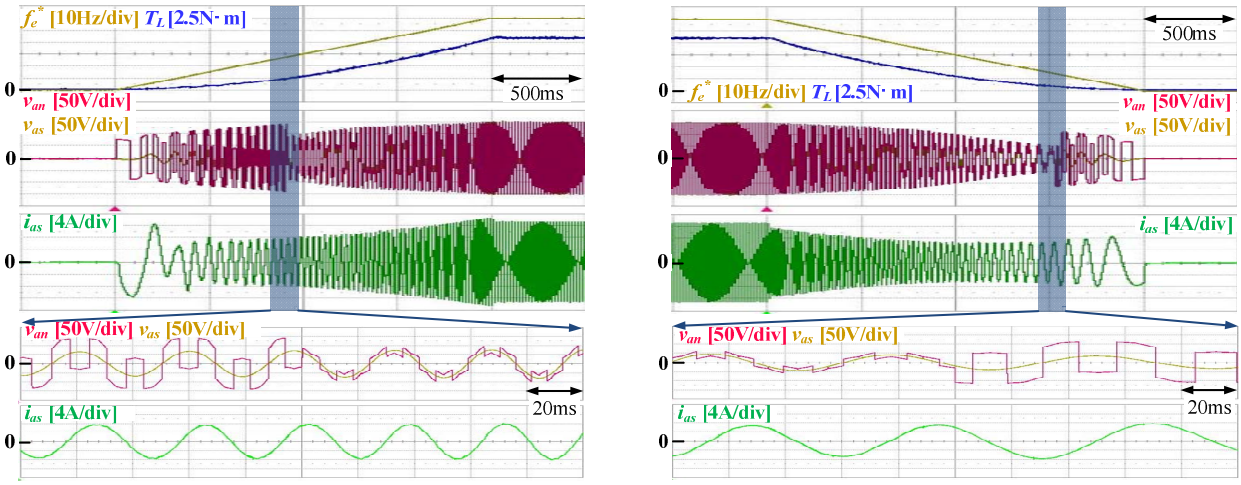


(c) v_{sn}^* in (7), compensation



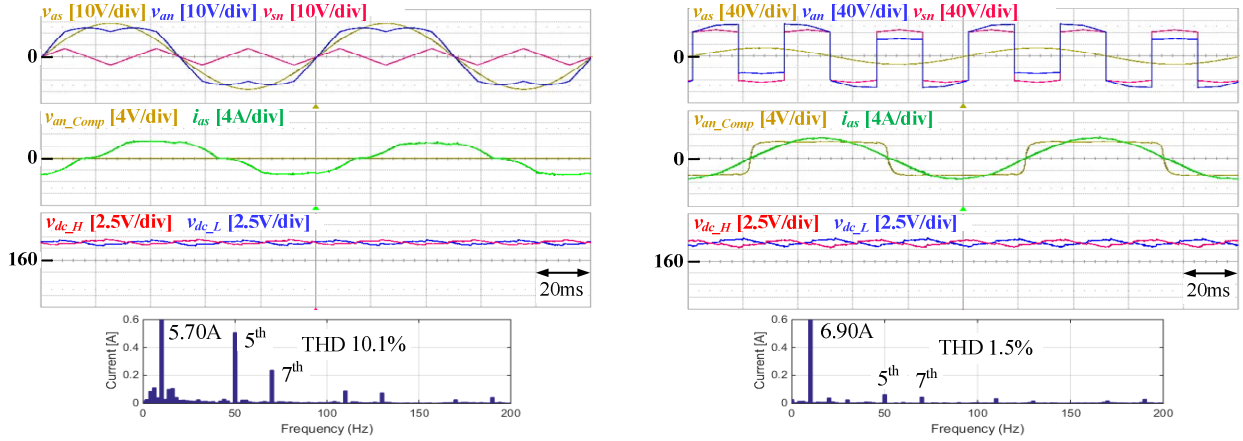
(d) AOVPWM, compensation

Fig. 15. Experiment 1: Waveforms and harmonic spectrum of i_{as} under no load, 10Hz frequency.



(a) Acceleration (b) Deceleration

Fig. 16. Experiment 2: Waveforms with mode transition under V/f operation.



(a) SCPWM, no compensation (b) AOVPWM, compensation

Fig. 17. Experiment 3: Waveforms and harmonic spectrum of i_{as} with NP controller under no load, 10Hz operating frequency.

The SMPMSM is controlled by a two-level inverter for applying load torque to the motor under the test. All control algorithms are implemented digitally in a DSP board. Each dc-link capacitance, switching frequency, and preset dead time are 4000μF, 10 kHz, and 3μs, respectively. The sampling frequency is set to 20 kHz.

A. Performance of inverter nonliearity comepnsation

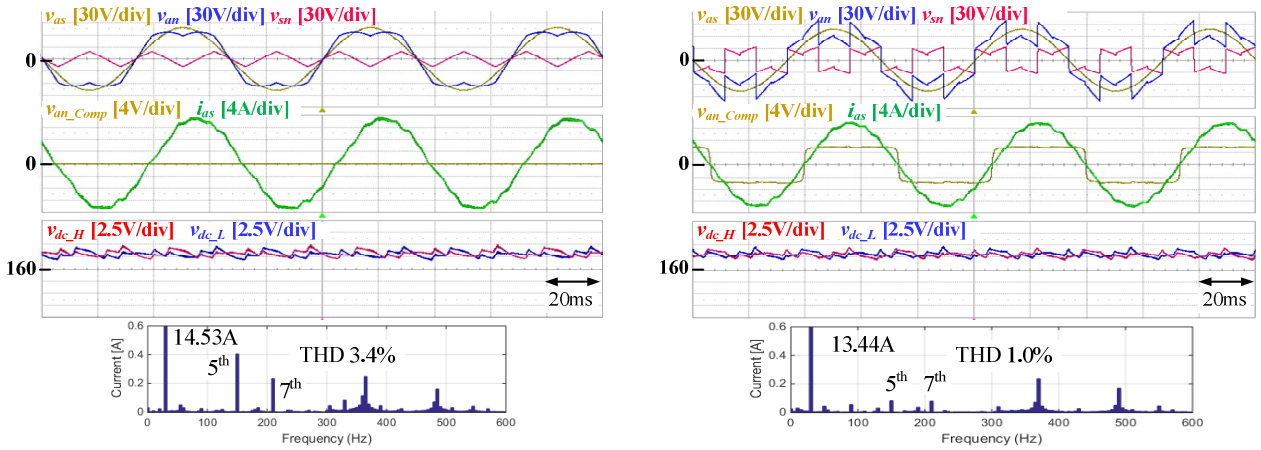
Fig. 15 shows waveform and harmonic spectrum of i_{as} according to PWM methods under no load and 10Hz operating frequency. Each dc-link voltage is fixed to 155V by a DC supply. In Fig. 15(a) where no compensation is applied, i_{as} is severely distorted due to the inverter nonlinearity. Even after applying the compensation method as shown in Fig. 15(b), 5th and 7th harmonics in i_{as} are not eliminated because the voltage disturbance induced by the dead zones can't be compensated. Applying v_{sn}^* in (7), 5th and 7th harmonics of the current are conspicuously reduced as shown in Fig. 15(c). However, additional even order harmonics arise in i_{as} due to the voltage disturbance induced by aforementioned asymmetric δv_{xn_SW}. Applying AOVPWM, thanks to alternatively shifted pole voltages, even order harmonics of the current are eliminated as shown in Fig. 15(d).

Fig. 16 shows the transition between the two proposed PWMs. The load torque is set to be proportional to the square of the rotational speed to emulate fan and pump load. During acceleration, PWM mode is changed from AOVPWM mode to OMPWM mode when v_{max}-v_{min} = $0.5V_{dc}$-$4V_{DZ}$ as shown in Fig. 16(a). Fig. 16(b) shows that OMPWM mode is changed to AOVPWM mode when v_{max}-v_{min} = $6V_{DZ}$. The transition points during acceleration and deceleration are set differently by applying hysteresis for stable transition. The distortion of the current is well compensated even at the transition point.

B. Effectiveness of NP balancing control

The dc-link capacitor is connected to line-to-line $220V_{rms}$ 60Hz grid through three-phase diode rectifier. NP current is controlled by the proposed NP controllers. When SCPWM is applied, NP controller for OMPWM excluding v_{mar} limiter is used to compare the performance of proposed algorithms. NP controller gain, ω_{vc} and $k_{np,v}$, are set to 1Hz and -0.5.

Fig. 17 shows the effectiveness of AOVPWM with θ_{bal} controller under no load and 10Hz operating frequency. In Fig. 17(a) where SCPWM is applied without the compensation, dc-link voltages are well balanced. However, i_{as} is severely distorted due to the inverter nonlinearity. Applying AOVPWM



(a) SCPWM, no compensation (b) OMPWM, compensation

Fig. 18. Experiment 4: Waveforms and harmonic spectrum of i_{as} with NP controller under full load, 30Hz operating frequency.

and the compensation method, 5th and 7th harmonics of the current are conspicuously reduced without losing the voltage balancing control performance as shown in Fig. 17(b).

Fig. 18 shows the effectiveness of OMPWM under full load torque and 30Hz operating frequency with $v_{sn,bal}$ controller. Using the proposed scheme, 5th and 7th harmonic components of i_{as} are remarkably reduced compared to those in Fig. 18(a), maintaining the voltage balancing control performance.

VI. Conclusion

In this paper, inverter nonlinearity effects in three-level T-type inverters have been analyzed. Also, a scheme consisting of PWM techniques and compensation method to alleviate inverter nonlinearity effects have been proposed. The nonlinear effects are classified two parts, namely, one due to dead time and the other one due to voltage drop of switching devices. The effects are addressed and the remedy against each part has been proposed and discussed. Also, NP controllers to keep the voltage balancing of dc-link are introduced to incorporate proposed PWM methods. Finally, the validity and effectiveness of the proposed scheme are verified by experimental results. Using the proposed AOVPWM and OMPWM, not only even harmonics but also 5th and 7th harmonic currents are remarkably reduced in three-level T-type inverter. In addition, NP voltage can be balanced with proposed NP controllers. The proposed scheme could be extended to multi-level and multi-leg topology.

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