Suppression of Circulating Current in Parallel Operation of Three-Level Converters

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Abstract— **The Zero Sequence Circulating Current (ZSCC) flows inevitably in parallel converters sharing common DC and AC sources. The currents flowing commonly in all converters increase losses and decrease the overall capacity of parallel converters. This paper proposes a simple and effective ZSCC suppression method based on the Space Vector PWM (SVPWM) method with the ZSCC controller. The zero sequence voltage for the proposed SVPWM is calculated based not on the phase voltage references, but on the grid voltage. The limit of linear modulation index of the converters with the proposed method is analyzed compared to other methods, and it is proven that the limit of linear modulation index can be maximized with the proposed method. The effectiveness of the proposed method has been verified through the experimental set-up consisted of the four parallel three-level converters. It has been confirmed that the ZSCC is well suppressed and larger linear modulation index is achieved at the same time with the proposed method. Moreover, the proposed control method does not require any communication between converters to suppress the ZSCC unlike the conventional methods.**

Keywords—Zero Sequence Circulating Current; Parallel Converters; Circulating Current Suppression; Limit of Linear Modulation Index; Voltage Utilization Rate;

I. INTRODUCTION

With the rapid growth of renewable energy markets over recent years, the grid-connected converters have become indispensable to interface the distributed generators with the grid. Though two-level converters are still dominant as a topology for the grid-connected converters, the three-level converters are getting popular by virtue of its higher efficiency and smaller filter size compared to those of two-level converters.

Meanwhile, if converters are operated in parallel, which is a form of modular structure, the efficiency at a light load would be enhanced by turning on-off each converter according to the load condition. Furthermore, the production and maintenance cost of overall converters would be also reduced [1]-[4]. To save the cost of the system in parallel converters, the converters usually share same DC and AC sources as shown in Fig. 1. However, in this case, a considerable amount of Zero Sequence Circulating Current (ZSCC) inevitably flows between the converters [5]-[9]. The ZSCC does not just lower the system's efficiency and overall capacity of the parallel converters but

also distorts the current, which causes EMI and harmonic problems. Therefore, it is desirable to minimize the ZSCC as much as possible.

Many researches have been carried out on the ZSCC control in parallel converters [5]-[12]. The PI type ZSCC controller was utilized to eliminate the ZSCC in most researches, and some of them presented the feed-forward control method to enhance the performance of the controller [10]-[12].

In this paper, an improved ZSCC suppression control method for parallel three-level converters is proposed. With the proposed control method, the ZSCC is almost perfectly suppressed even at transients or in the situation where the parallel converters transfer different amounts of active or reactive power from each other. This characteristic cannot be achieved with the ZSCC suppression control method based on the conventional SVPWM. Moreover, since the proposed control scheme does not require any communication between converters to control the ZSCC, the proposed controller is more scalable and reliable compared to the conventional controllers proposed in [10]-[12] which set zero sequence voltage through communications between converters. In addition, the limit of the linear modulation index of parallel converters according to each PWM method is analyzed. It is also verified that the limit of linear modulation index with the proposed method is larger than those of the conventional ZSCC suppression control methods.
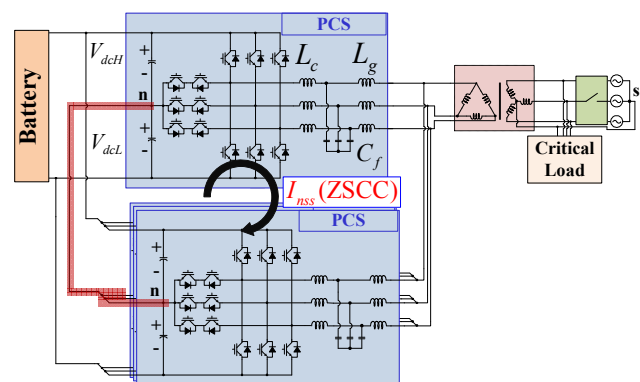

Figure 1. Four parallel three-level converters sharing common DC and AC sources.

II. ZSCC in Three-Level Parallel Converters

A. Zero Sequence Voltage and DC-link Voltage Balancing in Three-Level Converters

The ZSCC flows between parallel converters owing to the difference between the corresponding pole voltages of each converter. The difference naturally comes from a slight difference of the switching characteristics of each power semiconductor switches of converters even if the same gating signals have been applied to each converter. Due to the difference of the output filter impedances of the converters, the corresponding pole voltages of each converter would be different not only in transient state, but also in steady state to share equal portion of total load current. Because of these differences, the ZSCC would flow and the efficiency and total capacity of the converters would be degraded.

To suppress the ZSCC, several kinds of ZSCC controller have been used and the output of the ZSCC controller was added to the output voltages of the current regulator of each converter. The output voltages of the current controller of each converter would be different to regulate its own current, resulting in different phase voltage references for each converter. In this case, the Zero Sequence Voltage (ZSV) of each converter, defined as instantaneous average of the pole voltages of each converter, would be different under Space Vector PWM (SVPWM) and the ZSCC flows because of the difference in the ZSVs.

In converters with three-level topology, the ZSV of each converter also influences the balancing control of its DC-link voltage [13]. To set the ZSV for balancing the DC-link voltage equally while considering the suppression of the ZSCC, the upper capacitor voltage (V_{dcH}) and the lower capacitor voltage (V_{dcL}) of all the converters should be same respectively. For that reason, it is recommended that the DC-link neutral points of parallel converters be tied together as shown in Fig. 1 [14].

The ZSV for the DC-link balancing control can be set as (1).

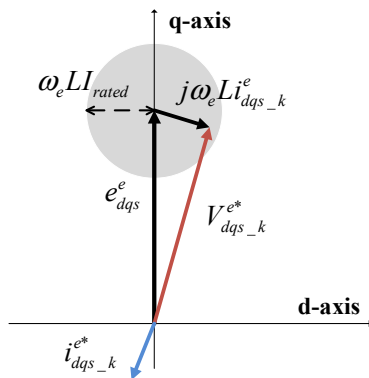$$V_{sn\_balancing} = sign(I_{qs}^{e*}) \frac{V_{dcH} - V_{dcL}}{2}. \qquad (1)$$

B. Relationship of the Output Power and ZSV

If the active power and reactive power references are set, the d, q-axes current references of each converter can be calculated. Then, d, q-axes voltage references of the k-th converter among n-parallel converters are determined as (2) in steady state.

$$V_{dqs\_k}^{e*} = j\omega_e L i_{dqs\_k}^{e*} + e_{dqs}^e, \quad where \ k = 1, 2, \cdots, n \qquad (2)$$

, where e_{dqs}^e and ω_e stand for the grid voltage and angular frequency, respectively, in d-q reference frame, and L for the summation of L_c and L_g in Fig. 1.

The active power and reactive power of parallel converters would be different not only in transient state, but also in steady state; because the filter inductances of the converters are different from each other due to tolerance of L, C components. These differences between the converters cause the difference in current references, which lead to the mismatch of the voltage references (V_{dqs_k}*) as shown in Fig. 2. If each converter uses the conventional SVPWM method, the ZSV of the k-th converter would be calculated as (3) based on its own voltage references (V_{dqs_k}*) [15]-[18].

$$V_{sn\_ff\_k} = -\frac{\max(V_{as\_k}^*, V_{bs\_k}^*, V_{cs\_k}^*) + \min(V_{as\_k}^*, V_{bs\_k}^*, V_{cs\_k}^*)}{2}. \qquad (3)$$

Finally, the different power references cause the different ZSVs, which are a main contributing factor of the ZSCC. To avoid different ZSVs, Sine PWM (SPWM), where no ZSV is used at the cost of 15% reduction of linear modulation index range, could be a candidate in the view-point of the ZSCC. However, 15% reduction of the linear modulation index range would not be tolerable in most cases of the applications.

C. Conventional Methods for Suppressing ZSCC

In general, the ZSCC has been suppressed by the zero-sequence current controller; to overcome the limited bandwidth of the zero-sequence controller, several methods using the feed-forward voltage, $V_{sn\_ff\_k}$, have been proposed as shown in Fig. 3 [10]-[12].
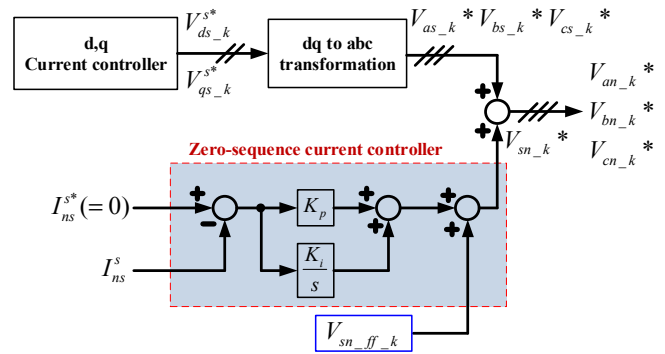

Figure 2. d, q-axes vector diagram of *k*-th parallel converter.

Figure 3. Zero sequence current controller of *k*-th parallel converter.

The ZSCC can be dramatically suppressed if all parallel converters use the identical V_{sn_ff}. V_{sn_ff} of all the converters can be set as the SVPWM ZSV of the master converter as (4) [10]. This method is termed as Method 1 (M1) in this paper. The other option for the identical V_{sn_ff} is the average value of the SVPWM ZSVs of the converters as (5), and this method is termed as Method 2 (M2) [11].

$$V_{sn\_ff\_M1} = -\frac{\max(V_{as\_master}^*, V_{bs\_master}^*, V_{cs\_master}^*) + \min(V_{as\_master}^*, V_{bs\_master}^*, V_{cs\_master}^*)}{2} \quad (4)$$

$$V_{sn\_ff\_M2} = -\frac{\sum_{k=1}^{n}\{\max(V_{as\_k}^*, V_{bs\_k}^*, V_{cs\_k}^*) + \min(V_{as\_k}^*, V_{bs\_k}^*, V_{cs\_k}^*)\}/2}{n} \quad (5)$$

III. PROPOSED ZSCC SUPRESSION METHOD

As mentioned in the previous section, the ZSV of each converter would be different from each other if the conventional SVPWM method is applied to all converters as in (3) [15]-[18]. Then, the ZSCC flows inevitably as described before. In this paper, the grid voltage, which are common to all parallel converters and the major portion of output voltages of current controller of each converter as seen from (2), are used for the calculation of the ZSV for SVPWM of each converter as (6). This method is termed as Grid based SVPWM (GSVPWM). Because all parallel converters are directly connected to the grid and measure the grid voltage for its own Phase Lock Loop (PLL), all converters would have the same ZSV with this arrangement.

$$V_{sn\_ff} = -\frac{\max(e_{as\_grid}^*, e_{bs\_grid}^*, e_{cs\_grid}^*) + \min(e_{as\_grid}^*, e_{bs\_grid}^*, e_{cs\_grid}^*)}{2} \quad (6)$$

To suppress the ZSCC, several methods such as M1, M2, and the method compensating the difference of zero vectors between converters have been introduced in [10]-[12]. But those are less scalable and reliable than GSVPWM due to the fact that the communication between converters at every sampling period is necessary for them to determine the feed-forward term of the zero sequence current controller (V_{sn_ff}).

IV. ANALYSIS OF VOLTAGE UTILIZATION RATE

In the case of SVPWM, the largest Limit of Linear Modulation Index (LLMI) of a single converter is considered as $\frac{2}{\sqrt{3}}$ [19], under the definition of the modulation index (MI) as (7).

$$MI \equiv \frac{|V_{as}|_{peak}}{V_{dc}/2} \quad (7)$$

The ZSCC would be shrunken if all parallel converters use the identical V_{sn_ff} like the cases of M1, M2, and GSVPWM. To have the capability of the ZSCC suppression, the LLMIs of those methods of converters are inevitably degraded compared to that of the independently operating converter based on SVPWM. However, the maximum LLMI of each method would be different. The ZSVs of M1, M2, and GSVPWM are

not based on their own phase voltage references so there exists angular and magnitude mismatch of ZSV between them and the conventional SVPWM.

Fig. 4 shows the LLMI according to the mismatch of the angle and magnitude from its conventional SVPWM ZSV. The angular mismatch of the SVPWM ZSV degrades the LLMI more than the mismatch on magnitude does. If the angular mismatch is larger than 15.5°, SVPWM where the ZSV is not based on each converter's own output voltages is no more superior to SPWM in the view point of the LLMI. The LLMI is the lowest at 60° angular mismatch as expected
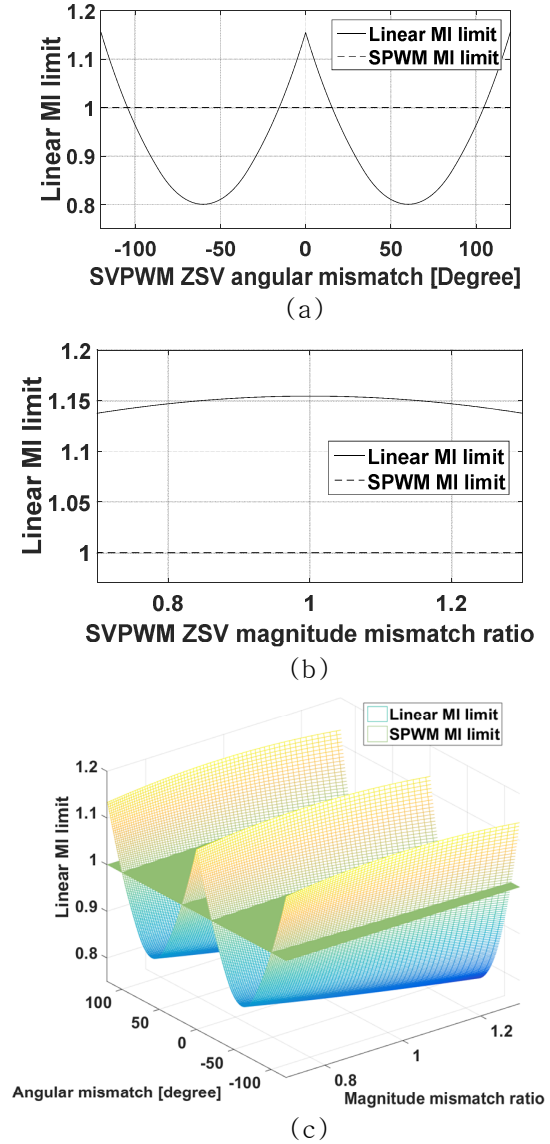

(a)

(b)

(c)

Figure 4. Linear modulation index limit (LLMI) (a) LLMI under angular mismatch without mismatch on magnitude, (b) LLMI under mismatch on magnitude without angular mismatch, and (c) three dimensional view of LLMI under angular mismatch and mismatch on magnitude.

Table I. Experimental Parameters.

Item	Value	Unit
S_{rated}	5	kVA
f_{sw}	5	kHz
$L_c + L_g$	0.075	$p.u.$
V_{ll_grid}	220	V_{rms}
I_{rated}	18.6	A_{peak}

Table II. LLMI according to V_{sn_ff}.

V_{sn_ff}	Maximum angular mismatch of ZSV	LLMI	Communication at each PWM sampling period
SPWM	0	1	No
M1	$2\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$	1.06	Yes
M2	$2\dfrac{n-1}{n}\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$	1.08 (when $n=4$)	Yes
GSVPWM	$\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$	1.11	No

because the phase voltage reference and the ZSV have the maximum values at the same moment.

In the following analysis, the LLMIs of M1, M2 and GSVPWM are compared. Prior to the analysis, it should be noted that the LLMI at the worst case of each PWM method determines the DC-link voltage at the system design stage to guarantee the satisfactory regulation of the grid current, and it consequently affects the cost of the converter and the reliability of the overall system.

If M1 is applied, the angular mismatch of the ZSV reaches up to $2\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$ where power references of one converter and another converter are rated values and have the opposite signs in the worst case transient. If M2 is applied, the angular mismatch can reach up to $2\dfrac{n-1}{n}\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$ in the worst case. With GSVPWM, the maximum angular mismatch in the worst case is $\tan^{-1}(\dfrac{\omega_e LI_{rated}}{V_{rated}})$.

With the parameters given in Table I, the LLMI of each method was calculated and listed in Table II. The voltage utilization rate of GSVPWM is superior compared to that of others. It can be noted that $V_{sn\_balancing}$ in (1) is neglected in above comparison since the magnitude of $V_{sn\_balancing}$ is much smaller than the magnitude of the ZSV.

V. EXPERIMENTAL RESULTS

The experimental set-up is implemented as Fig. 5. Four three-level T-type converters are connected in parallel between a battery bank and the grid in common, and the neutral points of three-level converters are tied together. The parameters of the experimental set-up are listed in Table I.

Fig. 6 (a) and (b) shows the A-phase total current (I_{as_total}), the upper capacitor voltage (V_{dcH}), the lower capacitor voltage (V_{dcL}), and the ZSCCs of all four converters (I_{zscc_PCS1}, I_{zscc_PCS2}, I_{zscc_PCS3}, I_{zscc_PCS4}) simultaneously. These four converters are connected to the grid in sequence with the rated power reference. When connecting to the grid, the power reference of each converter increases with limited slew rate, 0.2 p.u./s. In
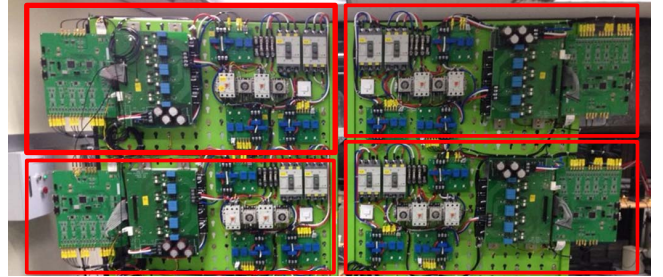
5 kVA PCS × 4

Figure 5. Experimental Setup: 5kVA Four Parallel three-level T-type Converters.

the case of the conventional SVPWM, which sets $V_{sn\_ff\_k}$ as (3), the difference of the power references causes the considerable ZSCC at transient as shown in Fig. 6 (a). The magnitude of the ZSCC of the converter lastly connected to the grid is the largest as shown in Fig. 6 (a), and it reaches up to 54% of the rated current of the converter. It should be definitely suppressed for the practical application of parallel converters. As shown in Fig. 6 (b), the ZSCC is well suppressed with the GSVPWM method which sets V_{sn_ff} as (6). In both PWM methods, the DC-link voltage is well balanced.

To be more specific, the waveform at the moment where PCS1 outputs the rated power (5kW), and PCS2 outputs zero power (0kW), was depicted in Fig. 7. This situation occurs when PCS2 just started switching while PCS1 was running.

Fig. 7 (a), (b), (c), and (d) show the ZSVs of PCS1 and PCS2 ($V_{sn\_ff\_PCS1}$, $V_{sn\_ff\_PCS2}$), the difference between the ZSVs of PCS1 and PCS2 ($V_{sn\_ff\_PCS1} - V_{sn\_ff\_PCS2}$), and the ZSCCs of PCS1 and PCS2 (I_{zscc_PCS1}, I_{zscc_PCS2}) simultaneously. As analyzed in II-B. and shown in Fig. 7 (a), different active power between parallel converters cause different ZSVs between converters and it inevitably generates ZSCCs. The dominant ZSV component is 3rd harmonic, and the ZSCC on PCS1 flows only into PCS2 since ZSCC cannot flow into the grid. With GSVPWM, the ZSCC is almost perfectly suppressed even in the situation where each PCS outputs totally different amounts of power as shown in Fig. 7 (b). These experimental results confirmed the previous analysis on the ZSCC which claimed that different ZSVs between parallel
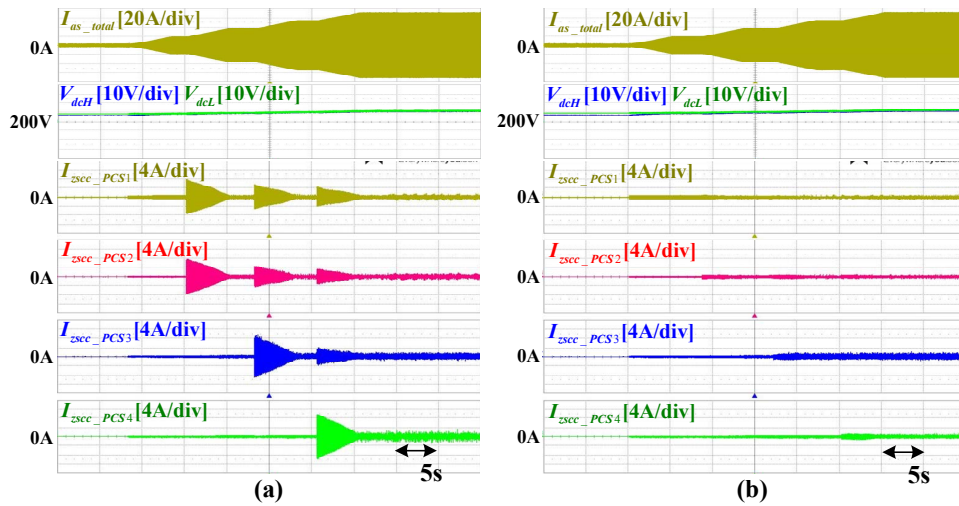
Figure 6. Experimental results – ZSCC (a) with the conventional SVPWM, and (b) with GSVPWM.
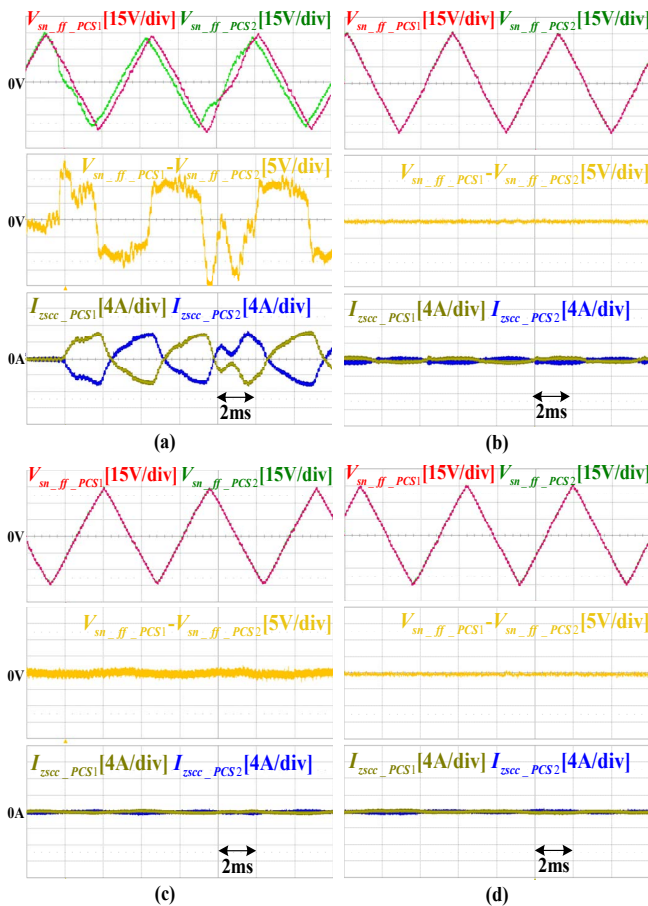

Figure 7. Experimental results – V_{sn_ff} and ZSCC (a) at transient with the conventional SVPWM, (b) at transient with the GSVPWM, (c) at steady state with the conventional SVPWM, and (d) at steady state with the GSVPWM.

converters are the source of ZSCC. As shown in Fig. 7 (c) and (d), the ZSCC at steady state is negligible in both the conventional SVPWM and GSVPWM.

It can be noted that M1 nor M2 could not be applied to the experimental parallel converter systems because both methods require communication between the converters at each PWM sampling period to transfer their common ZSV (V_{sn_ff}), but each experimental converter was made with the form of modular structure consists of a control board and a power board communicating each other through CAN (Controller Area Network). CAN, which is one of the most common communication system whose bandwidth is up to several Mbps, is insufficient to support the communication for M1 or M2. Since M1 and M2 with powerful communication capability, and GSVPWM method share the same ZSCC suppression principle, their ZSCC suppression performance would be the same. However, due to no need of powerful communication link between converters GSVPWM method is still meaningful because it is more scalable and reliable than M1 or M2.

VI. CONCLUSIONS

This paper has proposed a simple and effective ZSCC suppression method, which utilizes zero sequence controller with a feed-forward term. For enhanced linear modulation index range of the PWM, the ZSV for SVPWM in the proposed method has been calculated based on the grid voltage, which are common to all parallel converters and the major portion of the output voltages of the current regulator of each converter. Since the proposed method does not require any communication to suppress the ZSCC unlike the conventional methods, it can alleviate the burden of communication systems and enhance the scalability and reliability of overall system. To verify the validity of the proposed control method, the experiments have been conducted with four parallel three-level converters. Furthermore, the LLMIs with ZSCC controller were analyzed. According to the analysis, without

communication between converters, the proposed method can extend the LLMI by 3~11% compared to the conventional methods still keeping the ZSCC virtually null.

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