A Comprehensive AC Side Single Line to Ground Fault Ride Through Strategy of a Modular Multilevel Converter for HVDC System

Shenghui Cui[1], Hak-Jun Lee[2], Jae-Jung Jung[3], Younggi Lee[3], and Seung-Ki Sul[3]
E.ON Energy Research Center[1], Corporate Technology R&D Center[2], Dept. of Electrical and Computer Engineering[3]
RWTH Aachen University[1], LSIS[2], Seoul National University[3]
Aachen, Germany[1], Anyang-si, Korea[2], Seoul, Korea[3]
scui@eonerc.rwth-aachen.de, sulsk@plaza.snu.ac.kr

***Abstract*—The AC side Single Line to Ground (SLG) fault is one of the most frequent faults in power systems. And, in an HVDC system based on modular multilevel converter it calls for the fault ride through strategy to transmit maximum possible electricity during the fault to secure power system stability. It presents different characteristics of SLG faults at the voltage regulator side and the power dispatcher side. In this paper a comprehensive fault ride through strategy for AC side SLG fault occurred at both converters of the HVDC system is proposed. The proposed method presents fast dynamics and promises maximum possible electricity transmission during the faults. Voltage fluctuation and current overshoot in transmission line during SLG fault can be fully suppressed by the proposed method. Moreover, the proposed control strategy is free of inter-station communication and secures the reliability of HVDC transmission system. Validity of the proposed method is verified by simulation of a ±200kV, 400MW point-to-point HVDC system (216 sub-modules per arm).**

Keywords—modular multilevel converter, HVDC, fault ride through, communication, single line to ground fault, maximum power transmission

I. INTRODUCTION

Voltage Source Converter (VSC) for High Voltage Direct Current (HVDC) transmission is a promising solution for future smart grid which would integrate a great amount of renewable energy sources into the existing AC grid. For VSC-HVDC, compared to the conventional two level or three level converters, a Modular Multilevel Converter (MMC) is a competitive candidate and is attracting worldwide attentions. MMC presents many advantages such as very low harmonics, low dv/dt, modularity and simple scaling, high reliability and low switching loss, no necessity of series connection of power semiconductors, and the DC bus capacitor elimination [1-3], etc.

In a point-to-point VSC-HVDC transmission system, one station operates in the Voltage Regulator (VR) mode to regulate the HVDC transmission line voltage, and the other one operates in the Power Dispatcher (PD) mode to regulate the power that flows through the transmission line [4]. For practical application of MMC to HVDC, it calls for converter protection and fault ride through capability to improve system reliability. In the conventional point-to-point system control strategy, the direct modulation based control strategy was employed for each MMC [5-7]. Average voltage of the sub-module capacitor of MMC was imposed on the DC bus voltage of the MMC while the direct modulation was implemented [8-10]. Considering the SLG fault, main drawbacks of the conventional control method would be as follows. At first, in unbalanced grid condition such as a SLG fault, a twice line frequency oscillation is imposed on the DC bus voltage. The twice line frequency oscillation would not only be delivered to the other station resulting in additional voltage stress to the power semiconductors of MMC but also lead to malfunction of the protection system [7]. Several additional controllers are proposed to suppress such oscillation in case of unbalanced voltage conditions [7, 11-13]. Secondly, if a SLG fault occurs at the PD side while it operates at inverter mode to deliver active power to the coupled grid, the average sub-module capacitor voltage of MMC would rise abruptly causing temporary DC bus overvoltage since the average sub-module capacitor voltage is imposed simultaneously on the DC bus voltage [11].

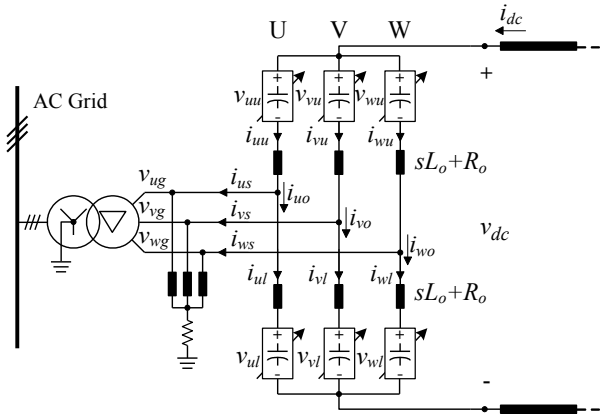


Fig. 1. Simplified schematic of the MMC converter station in HVDC application.

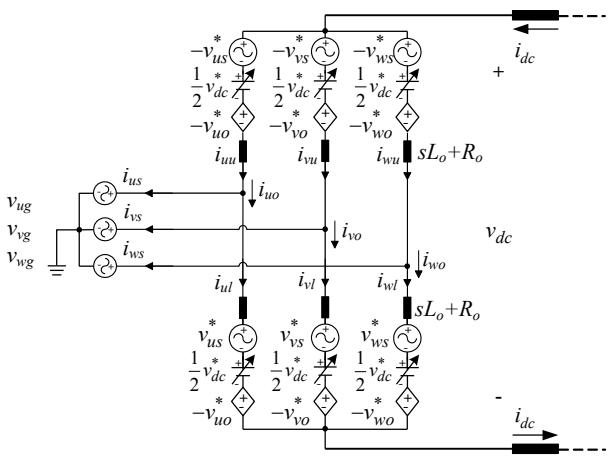


Fig. 2. MMC circuit for generalized DC bus if the indirect modulation is employed.

For an SLG fault, it's usually required to ride through the fault to transmit commanded power as long as possible. Since the magnitude of the positive sequence component of the faulted grid voltage decreases down to around 2/3 of the rated value during an SLG fault, conversion capability of the MMC that coupled with the faulted grid decreases temporarily due to limitation of converter AC side current capability. It would not be a challenging issue if the SLG fault occurs at the PD side since the power would be limited automatically by the current limiting block. However, while the fault occurs at the VR side, the VR converter would lose the controllability of the HVDC transmission line voltage if the PD keeps drawing the same power before the fault. Therefore a communication-free fault ride through strategy is essential to limit the transmission power during the SLG fault that occurs at the VR side to secure the stability of both the VR converter and the whole point-to-point system.

Several efforts had been done on this issue for VSC-HVDC systems based on two/three-level converters [14-15]. The fault ride through strategies can be generally classified into two types, respectively the Power Dispatcher Current Limiting (PDCL) strategy and the Power Dispatcher Mode Transition (PDMT) strategy. In the PDCL strategy [14], the PD converter had limited the AC side current as the available maximum value in accordance with the variation of the DC bus voltage. In the PDMT strategy [15], the PD converter had changed the operation mode from the PD mode to the VR mode while the DC bus voltage was out of the allowed range.

However, in the conventional strategies, voltage fluctuation and overcurrent would occur in the HVDC transmission line during the fault due to the inherent capacitor-inductor-capacitor coupling of the HVDC transmission line. The temporary overcurrent in the HVDC transmission line would not be a serious problem for the HVDC system based on two/three level converters since the DC current does not flow through the power semiconductors directly, rather flows through DC link capacitor. However, the overcurrent in the HVDC transmission line is not allowed for the MMC converter since the transmission line current flows through the power semiconductors directly in the MMC.

In this paper, a novel SLG fault ride through strategy for HVDC transmission system based on MMC is proposed. In the proposed method, transmission line voltage fluctuation is fully suppressed and the transmission line current is controlled actively without overcurrent during severe disturbances resulted from faults such as the SLG fault. Moreover, the proposed method secures the MMC capacitor energy regulation and guarantees the maximum possible electricity transmission without any inter-station communication during the SLG fault that occurs at the VR side.

II. Single Converter Control Strategy

A simplified schematic of the MMC converter station in the HVDC application is shown in Fig. 1. Typically, the MMC is grounded by a star reactor grounding device at transformer secondary side in HVDC application [16]. As the previous step of this work, a comprehensive MMC single converter control strategy based on indirect modulation was proposed [17].

The MMC circuit for generalized DC bus is shown in Fig. 2 if the indirect modulation technique is employed. Output voltage of each arm includes three parts, respectively the output AC voltage v_{xs}^* which is associated with AC grid current regulation, the DC bus command voltage v_{dc}^* with DC bus voltage synthesis, and the leg internal voltage v_{xo}^* with circulating current regulation. The leg current i_{xo} is defined as the mean value of upper and lower arm currents as (1).

$$i_{xo} = (i_{xu} + i_{xl})/2. \tag{1}$$

In [17], a universal MMC model under generalized nature of DC bus was proposed. In the proposed model that shown in Fig. 3, the MMC circuit in Fig. 2 can be divided into three equivalent circuits to describe respectively AC grid current, DC bus current, and the circulating current that defined as (2).

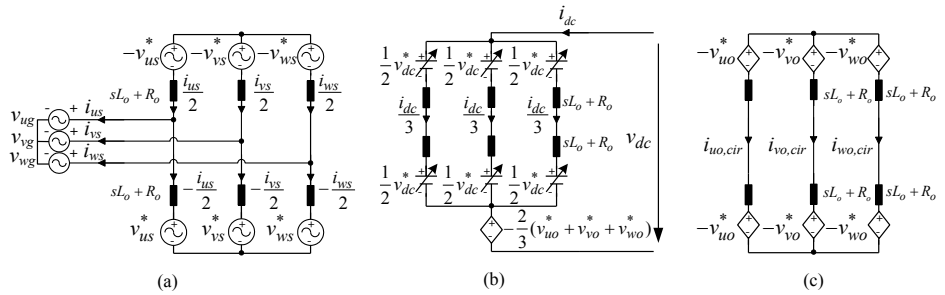
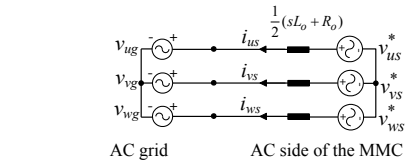
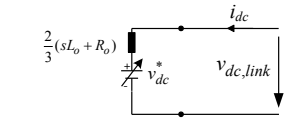


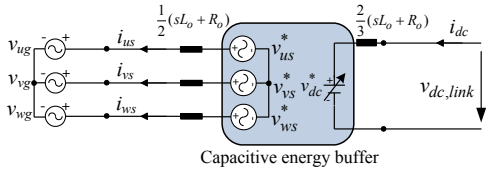
Fig. 3. Three equivalent circuits for the proposed universal MMC model under generalized nature of DC bus: (a) Equivalent circuit for AC grid current, (b) Equivalent circuit for DC bus current, (c) Equivalent circuit for circulating current.



(a) AC grid current model



(b) DC bus current model



(c) Model of the single MMC by the proposed control strategy

Fig. 4. Terminal modeling of the MMC controlled by the proposed single MMC control strategy.

$$i_{xo,cir} = i_{xo} - i_{dc}/3. \tag{2}$$

Based on the equivalent MMC model, a comprehensive arm capacitor energy balancing control strategy was proposed. One of the highlights of the proposed arm capacitor energy balancing method is that the capacitor energies of six arms of the MMC are balanced only by injection of the circulating current which only flows inside the MMC. Then the AC grid current, the DC bus current, and the arm capacitor energy balancing control are fully decoupled by the proposed method.

By the proposed indirect modulation based MMC control strategy, from the AC grid side the MMC looks like a three-phase controlled AC voltage source behind three phase inductors as shown in Fig. 4(a). And, from the DC transmission line side the MMC looks like a high bandwidth controlled DC voltage source behind an inductor as shown in Fig.4(b). It should be emphasized that the voltages of both the three-phase AC voltage source and the controlled DC bus voltage source can be updated in every sampling period of the digital controller by the proposed method (100μs order).

Generally, by the proposed MMC control strategy, the role of the half-bridge sub-modules is simply generating commanded three-phase AC voltage to the AC grid side and generating commanded DC voltage to the DC bus side. The

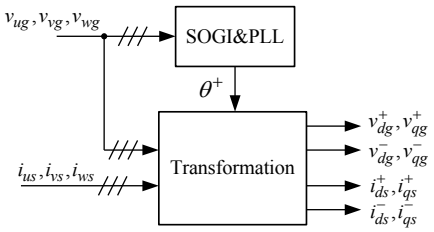


Fig. 6. Block diagram of the SOGI based PLL system to separate positive and negative sequence components of grid voltage and current.

capacitors of the sub-modules play a role of the capacitive energy buffer between the three-phase AC voltage source and the DC voltage source generated by the MMC itself as in Fig. 4(c). Then dynamics of the energy stored in the whole sub-module capacitors of the MMC can be described as (3) neglecting the losses of the system.

$$\frac{d}{dt}E_{total} = v_{dc}^{*}i_{dc} - (v_{us}^{*}i_{us} + +v_{vs}^{*}i_{vs} + v_{ws}^{*}i_{ws}). \tag{3}$$

III. System Control in Normal Operation

Based on the proposed single converter control method, a transmission system control strategy in normal operation was proposed [18]. Modeling of the transmission system where the MMC is controlled by the proposed single MMC control strategy is shown in Fig. 5. Different from the two/three level converter based HVDC system or the MMC-based HVDC system that controlled by the conventional direct modulation strategy, the VR converter generates constant voltage to the DC bus side by the high bandwidth controlled DC voltage source $v_{dc\_I}^{*}$ in Fig. 5 and the PD converter regulates the power flow by regulating the transmission line current i_{line} directly and actively by the high bandwidth controlled DC voltage source $v_{dc\_II}^{*}$ in the DC bus side.

To deal with the unbalanced grid condition, the Second Order Generalized Integrator (SOGI) based Phase Locked Loop (PLL) system [19] shown in Fig. 6 is employed to separate positive and negative sequence components of both grid voltage and current, and to detect the phase angle of the positive sequence component of the grid voltage. In this paper, the voltage vector of the AC grid is oriented to the q-axis of the synchronous rotating reference frame.

The block diagram of the capacitor energy controller and the plant model of the capacitor energy of the VR converter are shown in Fig. 7. The total capacitor energy stored in the sub-modules of VR is regulated by drawing the active power from the coupled AC grid. The power drawn by the HVDC transmission line is utilized as a feed-forwarding term to

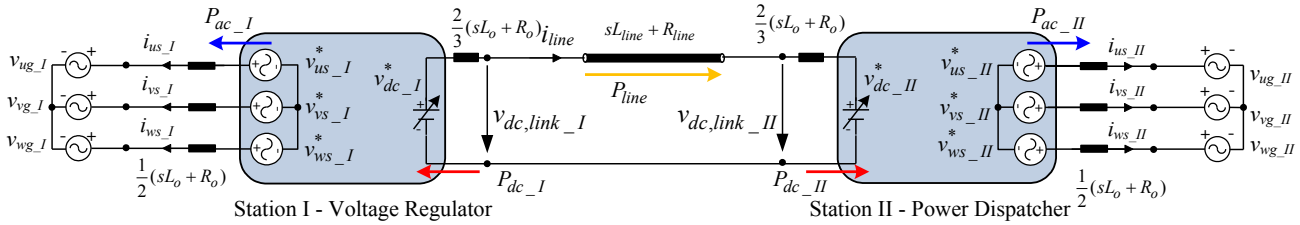
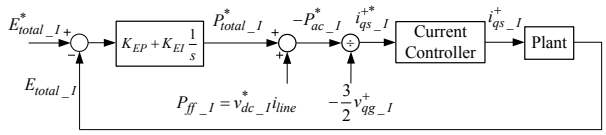
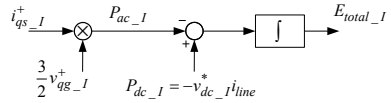


Fig. 5. Modeling of the HVDC transmission system where MMC is controlled by the proposed control strategy.

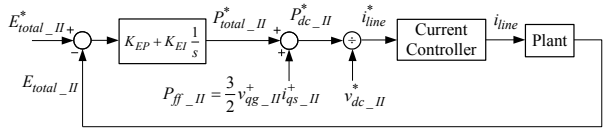


(a) Block diagram of the capacitor energy controller of the VR converter

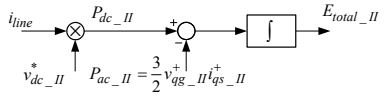


(b) Plant of the capacitor energy of the VR converter

Fig. 7. Block diagram of controller and plant of the capacitor energy of the VR converter.



(a) Block diagram of the capacitor energy controller of the PD converter



(b) Plant of the Capacitor energy of the PD converter

Fig. 8. Block diagram of controller and plant of the capacitor energy of the PD converter.

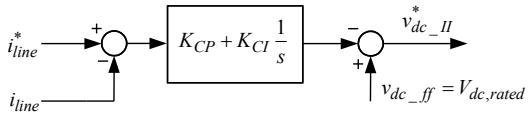


Fig. 9. Block diagram of the proposed transmission line current controller.

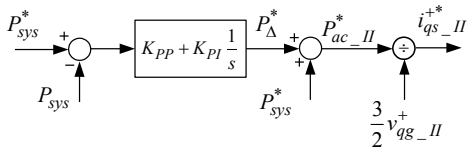
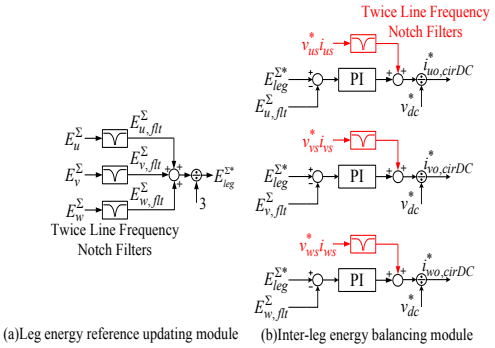


Fig. 10. Block diagram of the transmission line power flow controller installed in power dispatcher.



(a)Leg energy reference updating module (b)Inter-leg energy balancing module

Fig. 11. Block diagram of the modified leg capacitor energy balancing controller by injecting DC circulating current with feed-forwarding term.

improve the dynamic performance. In the normal operation, voltage of the controlled voltage source in DC side of the VR converter is synthesized constantly to the rated transmission line voltage as (4) to stabilize the transmission line voltage regardless of the total capacitor energy variation during the transient.

$$v^*_{dc\_I} = V_{dc,rated}. \tag{4}$$

The block diagram of the capacitor energy controller and the capacitor energy plant of the PD converter are shown in Fig. 8. The total capacitor energy stored in the sub-modules of PD is regulated by drawing the power from the HVDC transmission line. The power drawn from the transmission line is determined by the transmission line current i_{line} that controlled actively and directly by the high bandwidth controlled DC voltage source in the DC side of the PD converter, namely $v^*_{dc\_II}$ as shown in Fig. 9. Thanks to the active transmission line current control by the high bandwidth controlled voltage source, the fluctuations of transmission line voltage and current during rapid transient process can be fully suppressed [18].

The transmission line power flow controller installed in PD is shown in Fig. 10. The power flow is controlled by regulating the power that flows from the PD converter into the coupled AC grid in a closed-loop manner.

IV. Proposed SLG Fault Ride Through Strategy

A. Inter-leg Capacitor Energy Balancing

In the proposed MMC control strategy [17, 18], the leg capacitor energies (namely the energy stored in the sub-module capacitors of each leg) are balanced by injecting DC circulating current into the converter. Dynamics of leg capacitor energy are described by (5). While the AC grid is balanced, the active powers that flow from each leg into the AC grid are identical. Then in steady state there's no circulating current flowing inside the MMC since leg currents of three legs are the same.

$$\begin{cases} \dfrac{dE^{\Sigma}_{u}}{dt} = v^*_{dc}i_{uo} - v^*_{us}i_{us} = v^*_{dc}\left(i_{uo,cir} + \dfrac{i_{dc}}{3}\right) - v^*_{us}i_{us} \\ \dfrac{dE^{\Sigma}_{v}}{dt} = v^*_{dc}i_{vo} - v^*_{vs}i_{vs} = v^*_{dc}\left(i_{vo,cir} + \dfrac{i_{dc}}{3}\right) - v^*_{vs}i_{vs} \\ \dfrac{dE^{\Sigma}_{w}}{dt} = v^*_{dc}i_{wo} - v^*_{ws}i_{ws} = v^*_{dc}\left(i_{wo,cir} + \dfrac{i_{dc}}{3}\right) - v^*_{ws}i_{ws} \end{cases} . \tag{5}$$

A sudden active power unbalance would occur in case of the SLG fault due to the sudden grid voltage unbalance. Then as shown by (5), leg currents of three legs would differ from each other to maintain the leg capacitor energies of three phases at the rated value. It means that a DC circulating current would flow inside the converter continuously during the fault ride through to keep the leg capacitor energy balance. In this paper, a modified leg capacitor energy balancing controller, shown in Fig. 11, that based on the previous work is proposed to improve leg capacitor energy balancing dynamics in case of the sudden power unbalance.

The instantaneous power that flows out from the sub-module capacitors in a leg can be predicted by the product of reference voltage and measured current of the AC side controlled voltage source in Fig. 4(a). Then the predicted power can be utilized as a feed-forwarding term to improve the dynamics of leg capacitor energy balancing. Since there's a considerable twice line frequency fluctuation in AC side

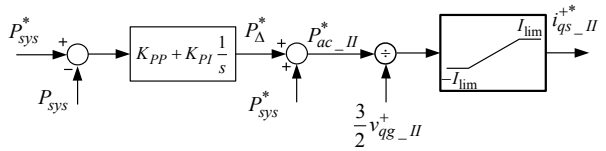


Fig. 12. Fault ride through control strategy for AC side SLG fault at PD converter.

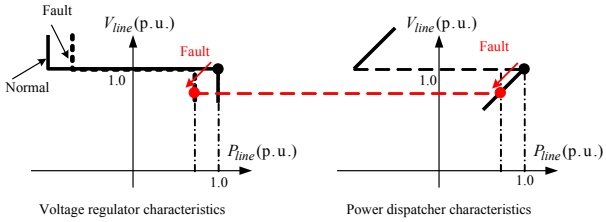


Fig. 13. Principles of power dispatcher current limiting strategy for fault ride through of the SLG fault at VR converter.

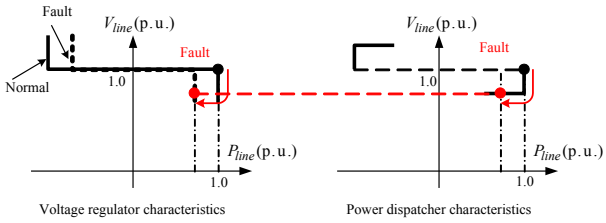


Fig. 14. Principles of power dispatcher mode transition strategy for fault ride through of the SLG fault at VR converter.

instantaneous power of each phase, notch filters are employed to filter out twice line frequency components. If the additional feed-forwarding term is not used, the integrators of the PI regulators in Fig. 11(b) would regulate the injected DC circulating current automatically to balance leg capacitor energy. However, it would lead to poor dynamic performance in case of the sudden power unbalance due to the fault. With the additional feed-forwarding term, the dynamic performance can be improved conspicuously.

B. SLG Fault at Power Dispatcher Side

The power capacity of the converter would decrease temporarily down to around 2/3 of the rated capacity during the SLG fault due to limitation of converter AC side current capability. While a SLG fault occurs at the PD side, it's simple to limit the power by adding a limiting block to the AC current reference since the PD converter regulates the power flow actively and the VR converter supplies the power passively.

If the magnitude of the transmitted power before the fault is smaller than the reduced PD conversion capacity during fault, then the magnitude of AC current of the PD would increase automatically to keep the power flow. However, if the magnitude of the transmitted power before the fault is larger than the reduced PD conversion capacity, then the magnitude of AC current of the PD would increase to the limiting value in Fig. 12 to transmit the possible maximum active power.

C. SLG Fault at Voltage Regulator Side

The VR converter plays a role of a DC power supply in the transmission system and its capacity would decrease in case of the SLG fault to around 2/3 of the rated power capacity. In

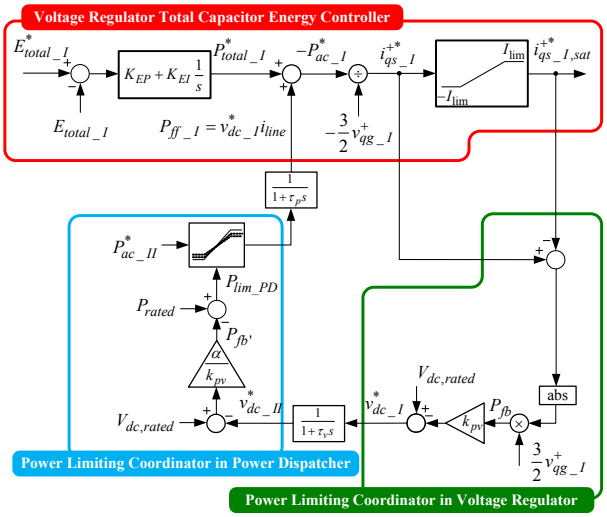


Fig. 15. Proposed fault ride through control strategy for AC side SLG fault at VR converter.

case of the AC side SLG fault at VR converter, coordination between the VR and PD converters should be employed to make the PD converter to decrease the power temporarily according to the reduced VR conversion capacity to ride through the fault still transmitting maximum available power. Additionally, such coordination would not be based on inter-station communication not to degrade the reliability of the system.

Several strategies have been proposed in the previous researches to deal with this issue [14-15]. In general, the conventional methods could be classified into the Power Dispatcher Current Limiting (PDCL) strategy and the Power Dispatcher Mode Transition (PDMT) strategy. In Fig. 13, the principles of PDCL strategy while the power dispatcher operates at inverter mode to deliver rated active power to the coupled grid are illustrated as an example. In VSC-HVDC system based on the two/three level converter or on the MMC in which the MMC is controlled by the conventional direct modulation strategy, dynamics of the DC bus voltage of the VR converter can be expressed as (6) [8,9].

$$\frac{d}{dt}\left(\frac{1}{2}C_{eq}v_{dc\_I}^2\right) = -\frac{3}{2}v_{qs\_I}^{+}i_{qs\_I}^{+} - P_{line}. \tag{6}$$

Since the magnitude of $i_{qs\_I}^{+}$ is limited to I_{lim}, the DC bus voltage of the VR converter would be out of control while the magnitude of the transmission line power is larger than the available maximum value. While a SLG fault occurs at the VR side, the threshold magnitude of the transmission line power that makes DC voltage of the VR out of control decreases to around 2/3 of the rated power as shown in Fig. 13. Then the DC bus voltage of the VR would decrease, and so does the DC bus voltage of the PD. Then PD decreases the active power that flows into the coupled AC grid automatically in accordance with the instantaneous DC bus voltage, and the transmission line would converge to another equilibrium point

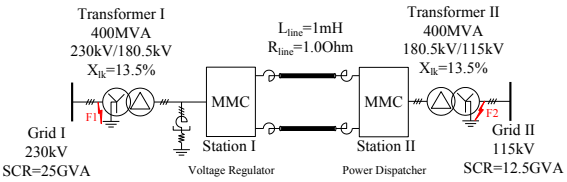
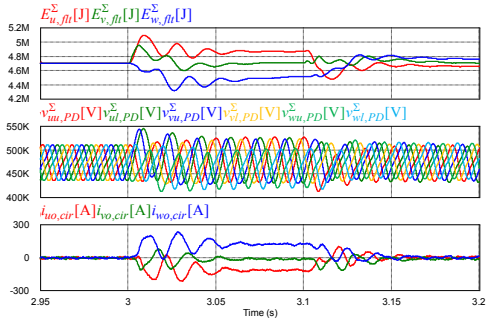


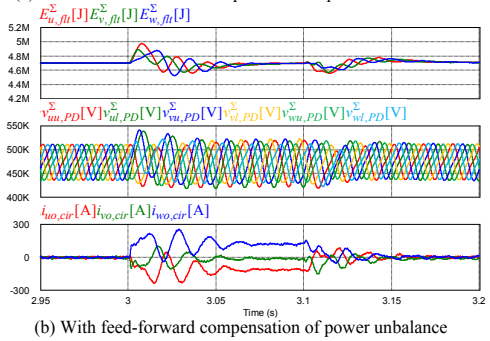
Fig. 16. Schematic of the simulated point-to-point HVDC system.

TABLE I. PARAMETERS OF THE SIMULATED SYSTEM

MMC converter	
Number of sub-modules per arm	216
Rated sub-module capacitor voltage	2.2kV
Sub-module capacitor	4.5mF
Inductance of arm inductor	15mH
Resistance of arm inductor	10mΩ
Controller sampling frequency	10kHz
Smoothing reactor	
Resistance	36mΩ
Inductance	10mH
HVDC transmission line	
Rated voltage	400kV
Rated current	1kA



(a) Without feed-forward compensation of power unbalance



(b) With feed-forward compensation of power unbalance

Fig. 17. Simulation results of leg capacitor energy balancing during SLG fault.(From top to bottom respectively leg capacitor energy of each phase , sum of sub-module capacitor voltages of each arm, and circulating current of each phase in PD)

where the voltages and powers of the DC buses of two converters coincide with each other.

In Fig. 14, principles of PDMT strategy while the power dispatcher operates at inverter mode to deliver rated active power are illustrated as an example. While a SLG fault occurs at VR side, the DC bus voltage of VR becomes out of control and decreases. Then the DC bus voltage of the PD decreases with that of the VR. When the DC bus voltage decreases to the threshold voltage, the PD would change operation mode from power dispatcher mode to voltage regulator mode. Then the DC bus voltage of PD would be clamped to the threshold voltage, and then the transmission line power would decrease to the maximum available power capacity of the VR at SLG fault condition to converge the system to a new equilibrium point.

There are several drawbacks that come with the conventional methods. At first, since there's an inherent capacitor-inductor-capacitor coupling in the transmission line and the transmission line current is passively determined by the power flow, an inrush current would occur during fast transient process such as the SLG fault. Secondly, the transmission line voltage has to be over the rated voltage while the power flows from the PD to the VR (namely P_{line} is negative.) as shown in Fig. 13 and Fig. 14. Moreover, some techniques should be employed to suppress twice line frequency oscillation in DC side of the MMC in case of the SLG fault.

Thanks to the proposed system control method, since the transmission line current is regulated actively and directly by the controlled DC voltage source in the DC bus of the PD converter, (7) would be always instantaneously guaranteed neglecting the voltage drop across the transmission line resistance, which is normally negligible.

$$v^*_{dc\_I} \approx v^*_{dc\_II}. \tag{7}$$

From (7), the VR converter can vary the voltage of the controlled DC voltage source, namely $v^*_{dc\_I}$ actively to notify the PD converter the lack of instantaneous conversion capacity in case of the SLG fault. As shown in Fig. 15 in the proposed strategy, the difference between the input and output values of the AC side current limiting block of the VR is exploited as a feedback signal to decrease the voltage of the controlled DC voltage source in VR converter. The power limiting coordinator in the VR converter codes the information of the difference between the instantaneous conversion capacity and the dispatched power P_{line}, namely P_{fb} in (8) to $v^*_{dc\_I}$.

$$P_{fb} = |P_{line}| - |P_{capacity}| = \left|\frac{3}{2}v^+_{qs\_I}i^{+*}_{qs\_I}\right| - \left|\frac{3}{2}v^+_{qs\_I}i^+_{qs\_I,sat}\right|. \tag{8}$$

While $v^*_{dc\_I}$ decreases, the output value of the transmission line current controller in the PD converter, namely $v^*_{dc\_II}$ would track $v^*_{dc\_I}$ automatically. The power limiting coordinator in power dispatcher then decodes the information to limit the dispatched power command in Fig. 10. Dynamics of the DC bus voltage of the VR when the conventional method is employed can be deduced as (9) from (6) by linearization, while dynamics of the DC bus voltage of the VR when the proposed method is employed can be deduced as (10) from Fig. 15.

$$|V_{dc,rated} - v_{dc\_I}| = \frac{1}{C_{eq}V_{dc,rated}}\int\left(\left|\frac{3}{2}v^+_{qs\_I}i^{+*}_{qs\_I}\right| - \left|\frac{3}{2}v^+_{qs\_I}I_{lim}\right|\right)dt. \tag{9}$$

$$V_{dc,rated} - v_{dc\_I} = k_{pv}\left(\left|\frac{3}{2}v^+_{qs\_I}i^{+*}_{qs\_I}\right| - \left|\frac{3}{2}v^+_{qs\_I}I_{lim}\right|\right). \tag{10}$$

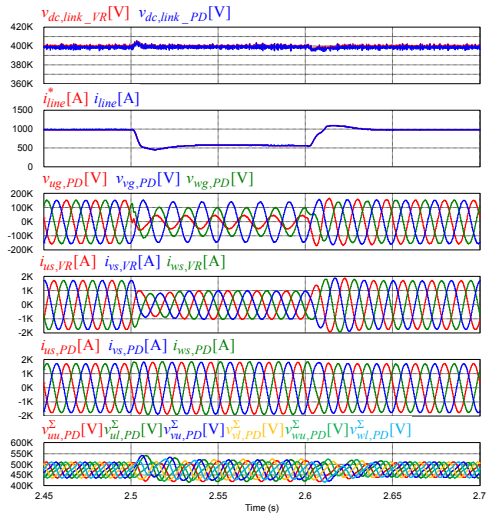


Fig. 18. Simulation results during SLG fault at PD side while P_{line} is 400MW.(From top to bottom respectively, DC link voltage of both converters, transmission line current and its reference value, secondary side voltage of the transformer connected with PD, AC side current of VR, AC side current of PD, sum of sub-module capacitor voltages of each arm in PD)

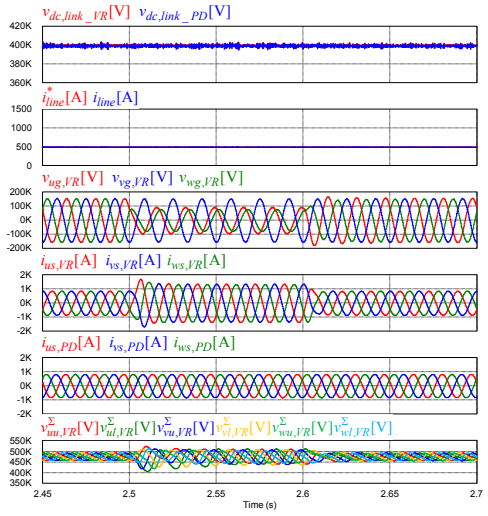


Fig. 19. Simulation results during SLG fault at VR side while P_{line} is 200MW.(From top to bottom respectively, DC link voltage of both converters, transmission line current and its reference value, secondary side voltage of the transformer connected with VR, AC side current of VR, AC side current of PD, sum of sub-module capacitor voltages of each arm in VR)

As shown clearly by (9) and (10), in the proposed method the DC link voltage variation is proportional to difference between instantaneous power capacity and the power that drawn by the transmission line, while in the conventional method the DC link voltage variation is proportional to integral of the difference, which would lead to a delay. Then compared to the conventional method, dynamic performance of the proposed method could be enhanced. Moreover, different from the conventional one, the transmission line voltage never goes over the rated voltage regardless of direction of the power flow. The proposed control strategy presents the following characteristics.

- The integrator in the VR total capacitor energy controller promises successful sub-module capacitor energy regulation during fault ride through.
- Since the power limiting coordinator in VR converter utilizes the difference between input and output values of the current limiting block, $v^*_{dc\_I}$ would not vary in normal operation or SLG fault at light load condition, where the magnitude of the AC current of VR is inside of the limiting block during the fault.
- If the magnitude of the transmitted power before the fault is larger than the reduced conversion capacity during fault, the integrator in the total capacitor energy controller of VR guarantees the maximum available power transmission in a closed-loop manner regardless of the transformer secondary side voltage variation due to the power variation.
- Overshoots of transmission line current and voltage are inherently avoided.

V. Simulation Results

To verify the proposed control strategy, a point-to-point VSC-HVDC transmission system shown in Fig. 16 is simulated by PSIM. A Thevenin equivalent method is employed to reduce simulation time without sacrificing accuracy [20]. The detailed parameters of the system are shown in Table. I. The transmission line current is limited in -1.1kA to 1.1kA. The AC current limit for the VR is set as 1900A and the AC current limit for the PD is set as 1820A.

A. Leg Capacitor Energy Balancing during Fault

Leg capacitor energy balancing performance during SLG fault has been investigated. A SLG fault occurs at PD converter at t=3.0s while the system is transmitting 400MW from the VR to the PD and is cleared at 3.1s. It can be shown in Fig. 17 that with the feed-forwarding compensation three leg capacitor energies can be balanced with much faster dynamics compared to the case without compensation. With the feed-forwarding compensation, DC circulating current is injected inside the converter as soon as the fault occurs to balance the leg capacitor energy. And, AC circulating current is also injected inside the converter at the beginning of the fault to balance upper and lower arm capacitor energy [17] but it vanishes after balancing. After the transient, only the DC circulating current flows inside the converter to compensate power unbalance and the circulating current vanishes after the clearance of the fault.

B. SLG Fault at Power Dispatcher Side

Fault ride through during the SLG fault at power dispatcher side is investigated. A SLG fault occurs at t=2.5s at PD side and is cleared after 0.1s while the system is delivering 400MW power, namely $P_{line} = 400\text{MW}$.

The PD side AC current increases to 1820A during the fault to transmit maximum available power and the transmission line current decreases due to power reduction as shown in Fig. 18. Different from the conventional control strategy of the MMC-based point-to-point HVDC system, no transmission line inrush voltage that caused by sudden power unbalance appears while the proposed method is employed and the twice line frequency oscillation in DC bus is inherently avoided.

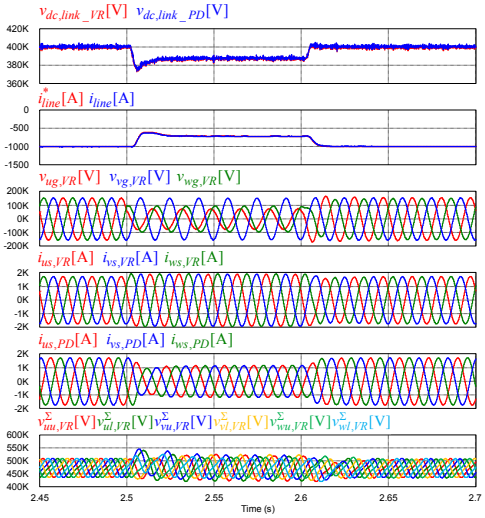


Fig. 20. Simulation results during SLG fault at VR side while P_{line} is -400MW.(From top to bottom respectively, DC link voltage of both converters, transmission line current and its reference value, secondary side voltage of the transformer connected with VR, AC side current of VR, AC side current of PD, sum of sub-module capacitor voltages of each arm in VR)

C. SLG Fault at Voltage Regulator Side

Fault ride through during the SLG fault at voltage regulator side is investigated. A SLG fault occurs at t=2.5s at VR side and is cleared after 0.1s.

The simulation results while P_{line} is 200MW are shown in Fig. 19. Since the power before fault is lower than the power capacity of the VR during the SLG fault, the power that flows through the HVDC transmission keeps constant during the fault, while the AC side current of the VR increases to maintain the power.

Fig. 20 shows simulation results while P_{line} is -400MW. It clearly demonstrates the difference with the conventional fault ride through strategies as follows. As the first, the transmission line voltage never rises over the rated voltage while a SLG fault occurs at VR side. As the second, the transmission line current is fully controlled to track its reference value. As the third, the inrush current during such rapid transient process is prevented.

From Fig. 18 to Fig. 20, arm capacitor voltages of six different arms are controlled at rated voltage with reasonably good dynamic performance when the proposed control method is employed.

VI. Conclusion

A communication-free novel SLG fault ride through strategy of the HVDC system based on MMC has been proposed in this paper. The proposed method guarantees the maximum available power transmission during fault ride through in a closed-loop manner. By the proposed method the sums of sub-module capacitor voltages of six arms are regulated to the rated value with fast enough dynamics after the fault occurs. The twice line frequency harmonics in the transmission line voltage during SLG fault is inherently avoided. The voltage fluctuation and current overshoot in the HVDC transmission line have been fully suppressed during transient by the proposed method. Validity of the proposed method was verified by simulation of a point-to-point HVDC system based on MMC employing 216 sub-modules per arm.

References

[1] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in Proc. IEEE Power Electronics Specialisits Conference, pp. 174-179, 2008.

[2] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in Conf. Rec. IEEE Transmission and Distribution Conference and Exposition, pp. 1-16, 2008.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. IEEE Boogna Power Tech, vol. 3, pp. 1-6, 2008.

[4] Lianxiang Tang, "Control and protection of multi-terminal DC transmission systems based on voltage-source converters," Ph.D dissertation, McGill University, Montreal, Quebec, Canada, 2003.

[5] Saeedifard M., Iravani R., "Dynamic performance of a modular multilevel back-to-back HVDC system", *IEEE Trans., on Power* Delivery, vol. 25, pp. 2903-2912, 2010.

[6] Q. R. Tu, Z. Xu, and L. Xu, "Reduced switching frequency modulation and circulating current suppression for modular multilevel converters," in IEEE Trans. Power Del., vol. 26, no. 3 ,pp. 2009-2017, Jul. 2011.

[7] Qingrui Tu, Zheng Xu, Yong Chang, and Li Guan, "Suppressing DC voltage ripples of MMC-HVDC under unbalanced grid conditions," *IEEE Trans. on Power Delivery*, vol. 27, pp. 1332-1338, 2012.

[8] Daniel C. Ludois, *et al*., "Simplified terminal behavioral model for a modular multilevel converter," IEEE Trans. on Power Electronics, vol. 29, pp. 1622-1631, 2014.

[9] Sheng Liu, *et al*., "Electromechanical transient modeling of modular multilevel converter based multi-terminal HVDC systems," IEEE Trans. on Power Systems, vol. 29, pp. 72-83, 2014.

[10] Firouz Badrkhani Ajaei, *et al*., "Enhanced equivalent model of the modular multilevel converter," *IEEE Trans. on Power Delivery*, vol. 30, pp. 666-673, 2015.

[11] Shaohua Li, *et al*., "Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Trans. on Power Electronics*, vol. 30, pp. 387-397, 2015.

[12] Ji-Woo Moon, *et al*., "Circulating current control in MMC under the unbalanced voltage," *IEEE Trans. on Power Delivery*, vol. 28, pp. 1952-1959, 2013.

[13] Yuebin Zhou, *et al*., "Analysis and control of modular multilevel converters under unbalanced conditions," *IEEE Trans. on Power Delivery*, vol. 28, pp. 1986-1995, 2013.

[14] Zhang Jing, "On control strategies for VSC-HVDC", Ph.D dissertation, College of Electrical Engineering, Zhejiang University, 2009.

[15] Chen Hairong, "Control and protection of VSC based HVDC system under AC system fault conditions," Ph.D dissertation, College of Electrical Engineering, Zhejiang University, 2007.

[16] C. Armschat, M. Dommaschk, V. Hussennether, T. Westerweller, "Star-point Reactor, " U.S. Patent US20120120691 A1, 2012.

[17] Shenghui Cui, *et al*., "A comprehensive cell capacitor energy control strategy of a modular multilevel converter (MMC) without a stiff DC bus voltage source," in *IEEE Applied Power Electronics Conference and Expo*., 2014, pp.602-609.

[18] Shenghui Cui, *et al*., "A novel control strategy of a modular multilevel converter (MMC) based VSC-HVDC transmission system," *IEEE Applied Power Electronics Conference and Expo*, 2015.

[19] P. Rodriguez, *et al*., "Multi-resonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. on Industrial Electronics*, 2010.

[20] U. Gnanarathna *et al*, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. On Power Delivery*, vol. 26, pp.316-324, 2011.