Electolytic Capacitorless 3-Level Inverter with Diode Front End for PMSM Drive

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***Abstract*—This paper proposes control of 3-level inverter with small DC-link capacitance and grid filter inductance for high speed motor drive system where regeneration and hold-up time are unnecessary. The controller consists of three simultaneously operating sub-controllers; High speed motor controller for flux weakening and maximum torque per ampere (MTPA) control, neutral voltage controller for DC-link voltage balancing, and active damping controller for DC-link stabilization. They are devised to operate in given DC-link voltage with their restricted voltage regions, avoiding interference among them. The analysis and design of each sub-controller and over all integration of them is discussed. The feasibility and performance of proposed control method is verified experimentally.**

Keywords—Motor drive, Capacitorless inverter, 3-level inverter, Active damping, Grid resonance.

I. INTRODUCTION

The current trend toward compact home appliances has been asking the way to its utmost efficiency and small passive components. The high efficiency benefits total system design through reduced cooling system size and cost as well as low running cost. The small passive components such as grid side inductance and DC-link capacitor used in drive system directly reduce system size but endanger system stability and grid code satisfaction.

A way to increase system efficiency may be the adaption of multi-level inverters, especially, 3-level T-type inverter which is known as the best efficiency [1]. Once, the application of the multilevel inverter to home appliance looked like prohibitive but thanks to the reduced cost of power semiconductors, the application of multilevel, especially T-type, is getting feasible. The reduced switching voltage of multi-level inverter decreases the core loss of target machine as well as switching loss of inverter itself. Furthermore, conduction loss of 3-level T-type inverter would be far less compared to that of conventional neutral clamped 3-level inverter. As mentioned, the additional burden of the cost is getting decreased as power semiconductor price is going down. But cost saving and performance enhancement from T-type inverter would grow as the reduction of the cooling system and passive elements such as DC-link capacitors and filter inductances. Especially, when the regeneration capability and hold-up time are unnecessary, which does in most of home appliances, DC link capacitor be further decreased. Moreover, small DC-link capacitor can be made of film capacitors which can increase the life time of whole system, conspicuously, compared to that with a bulk DC-link electrolytic capacitor [2].

There are groups of previous researches related to the control of aforementioned system. One group had dealt with high speed flux weakening control of Internal Permanent Magnet Synchronous Machine (IPMSM) concerning Modulation Index (MI), Maximum Torque Per Ampere (MTPA), and Power Factor (PF) [3-5]. The efficiency and performance of IPMSM depend on the flux weakening control method. Other group dealt with voltage balance control of 3-level inverter [6-9], generally with bulky DC-link capacitor. The floating neutral voltage of 3-level inverter can exceed the rated voltage of switching devices of the inverter causing them breakdown, and the possibility of breakdown becomes higher as DC-link capacitor is getting smaller. Hence, the voltage balancing control with extended control bandwidth is crucial for the 3-level inverter with small DC-link capacitance. The additional switching to address the control of neutral current was suggested [8-9] but it revealed that switching loss and voltage distortion due to dead time effect increased. The adaptive gain controlled with PI controller in [9] was not fast enough for the inverter whose current and voltage reference changes suddenly such as load change and resonance. The other group dealt with stabilization of DC-link voltage against positive feedback property comes from constant power operation of the inverter [10-15], especially for small DC-link capacitance. To enhance the stability a passive damping technique had been introduced in [11], while others suggested active damping control which injected a certain high-frequency voltage (active power) to its plant [12-15]. The typical active damping control estimates ideal DC-link voltage to generate its reference using sensors or observer [13-14]. However these controllers have needed grid parameters and shown delaying and recursive problems at high frequency with small DC-link capacitance and filter inductance. Using a high pass filter instead of sensor and observer was suggested [15-16] free from these issues. But the injection methods were not optimized, and analysis to the grid resonance with small grid filter was not presented.

This paper proposes a control method of 3-level inverter with small passive elements, i.e., grid filter inductance and DC-link capacitance. The previous researches had not considered the small grid filter system and they dealt the system as separated problems under their respective conditions; motor drive, neutral voltage balancing, DC-link stabilization. The controllers need to be modified for simultaneous operation under the voltage shortage as the back EMF of a motor running at high speed have to occupy most of available voltage within the hexagon boundary of PWM. The

Table 1. The operational parameters of the motor and inverter.

Operational Motor Parameters	Rated power	10.5 kW	Number of pole pair (pp)	3
	Rated torque	14 Nm	Phase resistance, R_s	0.1 Ω
	Rated speed	7200 r/min	D-axis inductance, L_d	3 ~ 2.6 mH
	Rated line voltage	380 V_{rms}	Q-axis inductance, L_q	5.8 ~ 4.4 mH
	Rated current	20 A_{rms}		
Inverter Parameters	Maximum DC-link voltage (at no load)	560 V	Each DC-link Capacitance, $2 \cdot C_{dc}$	47 μF
	Grid inductance, L_{gs}	30 μH	DC-link side filter inductance, $L_{g,dc}$	1 mH

(D-Q Inductance has its maximum near zero current and minimum at the rated current)

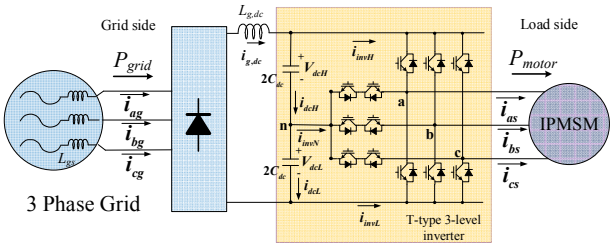

Fig. 1. 3-level T-type inverter with small passive elements.

feasibility and performance of modified control method to the balancing controller are verified analytically and experimentally through this paper

II. System Decomposition

The system under consideration is shown in Fig. 1 whose parameters are listed at Table 1. The system has a 3-phase AC source with grid source inductance, L_{gs}, a three phase diode rectifier, given DC-link inductance, $L_{g,dc}$, DC-link capacitor, C_{dc}, a 3-level inverter, and the IPMSM. The purpose of this system is to control the motor whose power only flows in from grid through diode rectifier to the voltage source PWM inverter. Unlike conventional systems with sufficient passive elements, every variable in the system such as grid-side DC-link current, $i_{dc,g}$, or DC-link capacitor voltage, V_{dc}, changes easily and should be kept to remain in certain range. There are only three controllable variables, which are 3-phase inverter output duties which are converted to synthesized output voltages in average during a switching period, V_{xn}, where x can be a, b, c. The three motor-side currents, i_{as}, i_{bs}, and i_{cs}, two series-connected DC-link capacitor voltages, V_{dcH} and V_{dcL}, and three grid currents, i_{ag}, i_{bg}, and i_{cg}, are variables to be controlled through the inverter output voltages.

The motor current has 2-dementional degree of freedom due to 3-phase 3- wire structure which has no common mode current. The low frequency components of voltage differences, i.e., line to line voltages, are used to control these motor currents with few hundreds Hz bandwidth performing speed or torque control. The voltage offset, V_{sn}, which does not affect line to line voltage and further to motor currents, is used for the control of the inverter neutral point current, i_{invN}, to balance voltage difference of DC-link capacitors, dV_{dc}, defined as the difference between V_{dcH} and V_{dcL}. The bandwidth of the balancing controller for the small DC link capacitance should be much faster than that for the bulk capacitance system not to break down switch elements due to overvoltage.

Furthermore, the total DC-link voltage, V_{dc}, sum of V_{dcH} and V_{dcL} and grid-side reveal a resonant response at a few kilo Hertz and resulting in instability due to inverter's positive feedback nature comes from the constant power operation of the inverter. The low-frequency ripple of DC-link voltage follows 3-phase rectified grid voltage which shows harmonics of 6th, 12th, 18th, and so on. The resonance between grid-side currents and DC-link capacitor voltage should be suppressed to satisfy grid-code, such as IEC 61000-3-12. The stabilization against positive feedback can be accomplished with an active damping control. The motor-side inverter drains undesired energy from DC-link and sends it to the motor. This high-frequency energy does not affect motor currents due to large motor inductance. Handling high-frequency energy, the active damping controller occupies high-frequency line voltage components.

The system can be modeled into three subsystems based on aforementioned system description; motor plant, DC-link voltage difference plant, grid-side and DC-link plant. This system decomposition is based on their different time constants. The typical fundamental motor current frequency is about a few hundred Hertz at most whose time constant is about 0.4ms at least as (1), where τ, ω, and f mean time constant, angular frequency and operating frequency respectively and subscript *fund* means corresponding variable is fundamental component. The time-constant of small DC link capacitor with a few micro-Farad capacitance would be around 0.1μs as (2), where R and C mean resistance and capacitor respectively and subscript DC means corresponding variable is DC-link component. The time constant of resonance between grid inductance of 1mH and few tens of microfarad DC-link capacitor is as (3), where L means inductance and subscript *res* and g means corresponding variable is resonance and grid-side components respectively.

$$\tau_{motor} = \frac{1}{\omega_{fund}} = \frac{1}{2\pi f_{fund}} \approx 0.44ms \,(if\ f_{fund} = 360Hz)\ . \quad (1)$$

$$\tau_{DC} = R_{dc}C_{dc} \approx 10^{-7}\, s \,(if\ R_{dc} = 5m\Omega, C_{dc} = 20\mu F)\ . \quad (2)$$

$$\tau_{res} = \frac{1}{2\pi f_{res}} = \sqrt{L_g C_{dc}} \approx 0.155ms\ . \quad (3)$$

III. Analysis and Design of Subsystem Controllers

A. IPMSM model and torque/speed control

The IPMSM motor plant is well-known as (4)–(5) [3], where λ, T_e, pp, ω_r, e, j, and subscript PM mean flux, motor

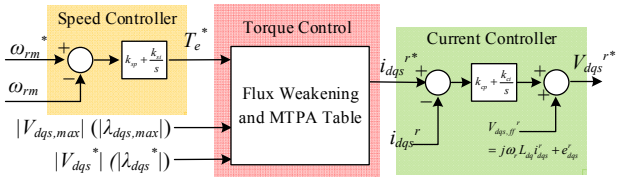

Fig. 2. Motor controller block diagram.

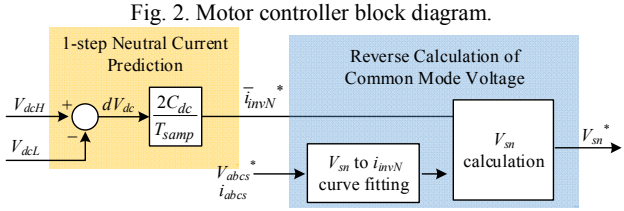

Fig. 3. DC-link voltage controller block diagram.

$$\lambda_{dqs}^{r} = (\lambda_{PM} + L_d i_{ds}^{r}) + jL_q i_{qs}^{r}.$$
$$V_{dqs}^{r} = R_s i_{dqs}^{r} + j\omega_r \lambda_{dqs}^{r} = R_s i_{dqs}^{r} + j\omega_r (L_{dq} \cdot i_{dqs}^{r}) + e_{dqs}^{r}. \quad (4)$$

$$T_e = \frac{3}{2} pp\left[\lambda_{PM} i_q + \left(L_d - L_q\right) i_d i_q\right]. \quad (5)$$

torque, number of pole pair, electrical rotating speed, back-electromagnetic force (EMF), complex unit space vector of dq-transform, and corresponding variable are of permanent magnet. Subscript *d*, *q*, and *s* mean corresponding variables are d axis, q axis, and motor variables respectively. Superscript *r* means corresponding variables are expressed in synchronous reference frame.

The control action of IPMSM consists of three stages as shown in Fig. 2; speed control, torque control, and current control. Speed controller is a PI controller in mechanical frame, and current controller is also a PI controller with feedforwarding tem , $V_{dqs,ff}^{r}$, in the rotor reference frame. The torque control of high speed IPMSM exploits negative d-axis current for dual purpose, namely, utilizing reluctance torque based on the inductance saliency known as MTPA and suppressing back-EMF known as flux weakening control. The MTPA control provides current reference with minimum copper loss at a given torque reference for an efficient operation of IMPSM. These flux weakening control and MTPA algorithm should be considered together, because both are subject to the voltage limitation of the inverter, so called as hexagon boundary. The torque control calls the least amount of d-axis current to suppress motor flux into PWM hexagon based on (4), followed by the decision of q-axis current to produce adequate torque based on (5). The table is usually used to map torque and voltage (flux) to currents as shown in Fig. 2, because the inductances of IPMSM strongly depend on operating current. $|V_{dqs,max}|$, $|\lambda_{dqs,max}|$, and superscript * stands for maximum available magnitude of output voltage of the current controller, V_{dqs}, for stator-side flux, λ_{dqs}, and for the reference value, respectively. The maximum available voltage, $|V_{dqs,max}|$, can be decided with the consideration of DC-link voltage. Hence, current reference varies with $|V_{dqs,max}|$, i.e., DC-link voltage, even at same torque reference. The high-speed IPMSM usually runs at utmost MI and about 0.9 PF for the maximum utilization of the capability of IPMSM under given limiting conditions. Generally the maximum available voltage, $|V_{dqs,max}|$, for flux weakening control is more than 95% of the inscribed circle of PWM hexagon as (6), and often more than 100% of the value with adequate over-modulation methods.

$$\left|V_{dqs,max}\right| = (modulation\ ratio)\frac{V_{dc}}{\sqrt{3}}. \quad (6)$$

In home appliance, the fundamental frequency of the output voltage of the inverter is much lower than switching (sampling) frequency, $f_{sw}=1/T_{sw}$, even for the high-speed machine.

B. DC-link voltage difference model and balancing control

The time constant of DC-link voltage with small DC link capacitance is much smaller than a switching period, whose typical value is larger than 20 μs. This makes the sampled capacitor voltages change in step manner in digital controller synced to switching frequency. The DC-link capacitor voltage difference, dV_{dc}, changes as (7) showing the voltage difference is only a function of neutral current during the switching period, where Δ means difference during a switching period, superscript $^-$ means average value, and the other variables are shown in Fig. 1.

$$\Delta dV_{dc} = \Delta V_{dcH} - \Delta V_{dcL} = \frac{T_{samp}}{2C_{dc}}(\bar{i}_{dcH} - \bar{i}_{dcL}) = \frac{T_{samp}}{2C_{dc}}\bar{i}_{invN}\ (during\ a\ switching\ period). \quad (7)$$

The neutral current and its average value can be calculated as (8)-(10), where *S* and *d* means switching state and duty factor respectively, and subscript *n* means corresponding variable is regarding neutral point, and the other variables are shown in Fig. 1.

$$i_{invN} = S_{an} i_{as} + S_{bn} i_{bs} + S_{cn} i_{cs} = \frac{1}{2}(2S_{an} - S_{bn} - S_{cn}) i_{ds} + \frac{\sqrt{3}}{2}(S_{bn} - S_{cn}) i_{qs}. \quad (8)$$

$$\bar{i}_{invN} = d_{an} i_{as} + d_{bn} i_{bs} + d_{cn} i_{cs} = \frac{1}{2}(2d_{an} - d_{bn} - d_{cn}) i_{ds} + \frac{\sqrt{3}}{2}(d_{bn} - d_{cn}) i_{qs}. \quad (9)$$

$$d_{xn} = \begin{cases} 1 - \dfrac{V_{xn} - V_{dc\_ref}}{V_{dcH}} = \dfrac{\frac{V_{dc}}{2} - V_{xn}}{V_{dcH}}, & if\ V_{xn} > V_{dc\_ref}. \\ 1 + \dfrac{V_{xn} - V_{dc\_ref}}{V_{dcL}} = \dfrac{\frac{V_{dc}}{2} + V_{xn}}{V_{dcL}}, & otherwise \end{cases} \quad (10)$$

$$V_{dc\_ref} = \frac{-V_{dcH} + V_{dcL}}{2},\ V_{xn} = V_{xs} + V_{sn}.$$

The duty factors decide average neutral current. Therefore, the common mode voltage, V_{sn}, which affects the duty factors, can be employed to control neutral current and balance DC-link capacitor voltages. The balancing control of DC-link capacitor voltages consists of two stages as shown in Fig. 3.

First stage is the calculation of adequate neutral current from voltage difference based on (7). The second stage calculates common mode voltage to flow neutral current as commanded at the first stage. The possible neutral current curve depends on the inverter line to line voltages and phase currents at instant, which are already decided for the motor control. After fitting the curve, adequate common mode voltage can be chosen. However, this reverse calculation often fails to find out the common mode voltage which makes the desired neutral current flow. Conventional researches uncovered the worst amount of accumulated charge according to MI and PF, i.e. steady AC line to line voltage and current [6]. At medium vector (high MI) with low PF where there is no way to control neutral current, DC-link capacitor voltage difference, dV_{dc}, would diverse in a few switching period with the small capacitance.

Additional voltage distortion can occur during switching period as neutral currents flows in and out even proper common mode voltage is chosen to flow zero neutral current in average. The dead time effect distorts duty factors from intended values and this also affects neutral current and causes voltage unbalance. The sampling delay and PWM synthesis delay shifts neutral current from commanded value to another. The resonance between grid and DC-link changes DC-link voltage and the fitting curve to find common mode voltage in that delay. This problem becomes worse with the small grid filter inductance as resonance frequency becomes higher. Although voltage unbalance from these reasons is inevitable, balancing control can keep the unbalance within certain range.

C. Grid current and DC-link voltage model and active damping control

The 3-phase grid-side and DC-link can be simplified to DC circuit with equivalent voltage source which describes rectified 3-phase grid voltage as shown in Fig. 4. The diode rectifier switch patterns are automatically decided according to comparison among grid voltages and DC-link voltage. The grid currents are a function of grid-side DC-link current, $i_{dc,g}$, with the diode rectifiers' switching patterns. Hence, grid-side currents control for satisfaction of grid-code is equivalent to DC-link voltage, V_{dc}, and grid-side DC-link current, $i_{dc,g}$, control with given 3-phase grid voltage, i.e., diode rectified grid voltage, $V_{g,eq}$, shown in Fig. 4. The diode rectified DC-link voltage has six peaks and valleys for every period of grid voltage (16.67ms for 60Hz) due to small DC-link capacitor. At the valley, the voltage is 87% of the peak and the average voltage in a period is about 95% of the peak. The equivalent resistance, $R_{g,eq}$, and inductance, $L_{g,eq}$, can be deduced as (11) [15], where subscript *g,ac* and *g,dc* means corresponding variables are regarding AC-side and DC-link side respectively. The last term right side of (11) is for voltage drop due to overlap angle of the commutation.

$$R_{g,eq} = 2R_{g,ac} + R_{g,dc} + \frac{3\omega_g L_{g,ac}}{\pi}. \qquad (11)$$
$$L_{g,eq} = 2L_{g,ac} + L_{g,dc}.$$

The DC-link capacitor voltages are assumed be balanced in

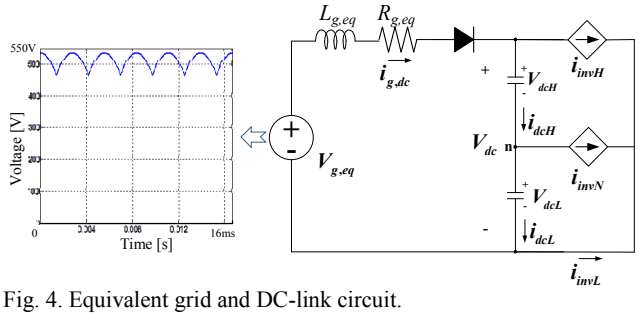

Fig. 4. Equivalent grid and DC-link circuit.

this model whose time constant is much slower than aforementioned balancing control. This is that neutral current is seen as zero and circuit equations are derived as (12)-(13).

$$V_{g,eq} = R_{g,eq} i_{g,dc} + L_{g,eq} \frac{d}{dt} i_{g,dc} + V_{dc}. \qquad (12)$$

$$i_{g,dc} = C_{dc} \frac{d}{dt} V_{dc} - i_{invH} \ . \qquad (13)$$

Small signal equation for the stability with constant inverter power consumption, P_{inv}, results in (14), where subscript *0* and superscript ~ means corresponding variables are regarding base value of small signal analysis and high frequency component respectively.

$$\frac{d}{dt}\tilde{V}_{dc} = 1/C_{dc}\left(\tilde{i}_{g,dc} - \frac{P_{inv}}{V_{dc0} + \tilde{V}_{dc}}\right) \approx 1/C_{dc}\left(\tilde{i}_{g,dc} + \frac{P_{inv}}{v_{dc0}^2}\tilde{V}_{dc}\right). \qquad (14)$$

$$\frac{d}{dt}\tilde{i}_{g,dc} = 1/L_{g,eq}\left(-\tilde{V}_{dc} - R_{g,eq}\tilde{i}_{g,dc}\right) \ . \qquad (15)$$

The last term of right side of (14) is a positive feedback term which can cause instability issue. This positive feedback comes from constant power consumption through the inverter regardless of DC-link voltage. On the other hand, the grid current behaves to stabilize DC-link capacitor against inverter's positive feedback properties. The passive stability criterion from (14) and (15) can be found out as (16) which cannot be satisfied with small capacitance in DC link.

$$\frac{C_{dc}}{P_{inv}} > \frac{L_{g,eq}}{R_{g,eq} v_{dc0}} \approx 20\frac{\mu F}{kW}. \qquad (16)$$

This instability from the positive feedback can be covered with an active damping control, which flows additional high frequency inverter current, $i_{invH,damp}$, to remove positive feedback term of (17) [13]. This additional inverter current shapes stability criterion to be always satisfied regardless of capacitance as (18) when the control variable, k_{damp}, is greater than or equal to unity.

$$i_{invH,damp} = -k_{damp}\frac{P_{inv}}{v_{dc0}^2}\tilde{V}_{dc}. \qquad (17)$$

$$\frac{C_{dc}}{P_{inv}} > 0 \geq \frac{(1-k)L_{g,eq}}{R_{g,eq} v_{dc0}} (if\ k \geq 1) \ . \qquad (18)$$

Although the positive feedback term is canceled out with the active damping and small signal stability is acquired, still there remains resonance problem between grid current and capacitor voltage as (19). The resistance, $R_{ac,eq}$, is a kind of

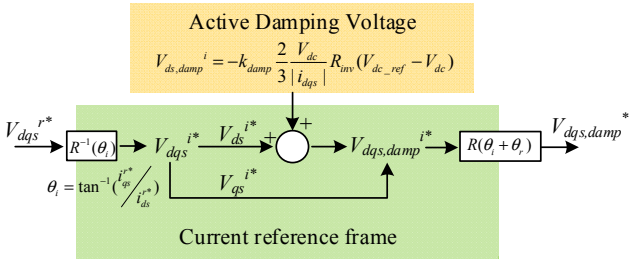

Fig. 5. Active damping controller block diagram

stray components which are generally not enough to damp the resonant out. The grid resonance frequency, f_{res}, is given by (20).

$$\frac{d}{dt}\tilde{V}_{dc} \approx {}^{1}\!/_{C_{dc}}\,\tilde{i}_{g,dc}\cdot$$
$$\frac{d}{dt}\tilde{i}_{g,dc} = {}^{1}\!/_{L_{g,eq}}(-\tilde{V}_{dc} - R_{g,eq}\tilde{i}_{g,dc}) \approx -{}^{1}\!/_{L_{g,eq}}\,\tilde{V}_{dc}\cdot \tag{19}$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{g,eq}\cdot C_{dc}}}\,. \tag{20}$$

This resonance problem can be subdued with the inverter damping current. The transfer function from inverter damping current, $i_{invH,damp,}$ to DC-link voltage can be derived as (21) from (19). This transfer function shows no phase delay at resonance frequency. Hence, voltage oscillation of resonance frequency can be suppressed with a proper damping current whose phase is same to the DC-link resonance voltage.

$$\frac{\tilde{V}_{dc}}{\tilde{i}_{invH}} = \frac{L_{g,eq}s + R_{g,eq}}{L_{g,eq}C_{dc}s^2 + R_{g,eq}L_{g,eq}s + 1}$$
$$\approx \frac{L_{g,eq}s + R_{g,eq}}{R_{g,eq}L_{g,eq}s} \approx \frac{1}{R_{g,eq}}(near\ f_{res}). \tag{21}$$

Conventional active damping control using actual DC-link voltage in the damping current calculation cannot generate proper damping current due to recursive and non-linear transfer function between base voltage, V_{dc0}, and actual DC-link voltage. The problem comes from the need of base voltage estimation and its delay. As the resonance frequency becomes higher with smaller grid filter inductance, phase relative delay due to estimation becomes larger. The proposed active damping control generates damping current reference as (22) without estimation. The first term of damping current, $i_{invH,damp}$, is to cancel out positive feedback term and the last term to suppress the resonance. The 1st voltage reference, $V_{dc,ref1}$, is set as average DC-link voltage and 2nd voltage reference $V_{dc,ref2}$, is set as desired DC-link voltage, for example, ideal diode-rectified grid voltage in Fig. 4.

$$i_{invH,damp} = -k_{damp}\frac{P_{inv}}{V_{dc,ref1}{}^{2}}(V_{dc,ref2} - V_{dc}).$$
$$\approx -\frac{P_{inv}}{v_{dc0}{}^{2}}\tilde{V}_{dc} + (1-k_{damp})\frac{P_{inv}}{V_{dc,ref1}{}^{2}}(V_{dc,ref2} - V_{dc}). \tag{22}$$

The transfer function from desired DC-link voltage reference, $V_{dc,ref2}$, to DC-link voltage is derived as (23). At resonance frequency, phase delay is zero but the magnitude of the transfer function is quite lower than unity. The unity transfer only can be achieved with large k_{damp}, because equivalent inverter resister, R_{inv}, is not a control variable which depends on inverter power consumption and average DC-link voltage.

$$\frac{\tilde{V}_{dc}}{V_{dc,ref2}} = \frac{{}^{\tilde{V}_{dc}}\!/_{\tilde{i}_{inv}}\,{}^{(1-k_{damp})}\!/_{R_{inv}}}{{}^{\tilde{V}_{dc}}\!/_{\tilde{i}_{inv}}\,{}^{(1-k_{damp})}\!/_{R_{inv}} - 1};\left(R_{inv} = \frac{V_{dc,ref1}{}^{2}}{P_{inv}}\right)$$
$$= \frac{(L_{g,eq}s + R_{g,eq})\,{}^{(k_{damp}-1)}\!/_{R_{inv}}}{(L_{g,eq}C_{dc}s^2 + R_{g,eq}L_{g,eq}s + 1) + (L_{g,eq}s + R_{g,eq})\,{}^{(k_{damp}-1)}\!/_{R_{inv}}}$$
$$\approx \frac{j7\,{}^{(k_{damp}-1)}\!/_{R_{inv}}}{j0.7 + j7\,{}^{(k_{damp}-1)}\!/_{R_{inv}}}(at\ f_{res}). \tag{23}$$

Flowing the active damping current can be achieved with high frequency power flow control from DC-link to the inverter. The low frequency power flow is already used for motor drive and the resonance frequency is higher than motor fundamental frequency. High frequency power flow control is achieved through adequate injection of high frequency voltage, $V_{dqs,dqmp}$ as (24), because current controller of that frequency is hard to be achieved. Moreover, motor current can be assumed to be constant in viewpoint of high frequency voltage, because the variation of the motor current in fundamental components is much slower than that of injected voltage. The injected voltage vector has the same direction to current vector for the least injected voltage magnitude as (25) [13], which is shown in Fig. 5, where $R(\cdot)$, θ, superscript ^{i} mean rotational vector, angle, and corresponding variable is at the current reference frame. Larger k_{damp} for the unity gain and null phase delay of the transfer function, (23), means larger injection voltage and energy for the active damping control.

$$V_{dc}i_{damp,invH} = P_{damp} = \frac{3}{2}V_{dqs,damp}\cdot i_{dqs} \tag{24}$$

$$V_{ds,damp}{}^{i} = -k_{damp}\frac{2}{3}\frac{V_{dc}}{|i_{dqs}|}R_{inv}(V_{dc\_ref} - V_{dc}) \tag{25}$$

IV. Overall Controller Design

A. Controller intergration with voltage sharing

The 3-level inverter with small passive elements for high-speed IPMSM drive needs aforementioned three controllers simultaneously operating. The overall integration of the sub-controllers should be done properly under the consideration of the operation of each sub-controller. The overall structure of the controller is depicted in shown in Fig. 6. The controllers output voltages and their sum is shown in Fig. 7. The motor controller output voltage, V^{r}_{dqs}, and the active damping controller output voltage, $V^{r}_{dqs,damp}$, are in synchronously rotating d-q frame. The motor control voltage could be considered as constant in the steady state, while active damping voltage, whose direction is same to motor current

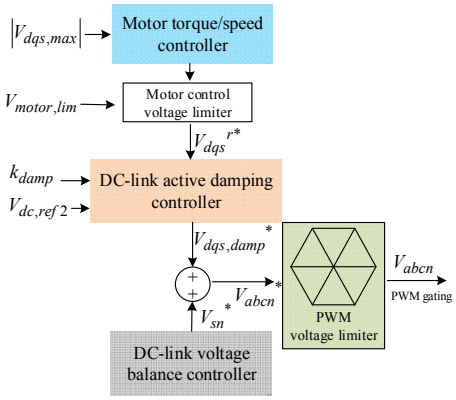

Fig. 6. Block diagram of overall integrated controller

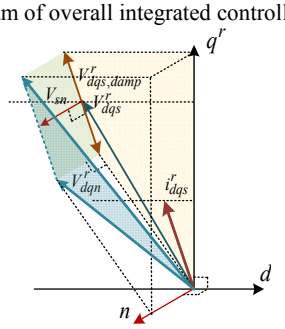

Fig. 7. Controllers voltage vector summation diagram

Table 2. The integrated controller design parameters

$\|V_{dqs,max}\|_{min}$	170V (0.87 PF)	$dV_{dc,max}$	150V
$\|V_{dqs,max}\|_{max}$	300V (0.9 PF)	$V_{dc,res,max}$	30V
$\|V_{dqs,max}\|_{dc,min}$	260V	k_{damp}	3
$\|V_{dqs,max}\|_{des}$	265V (0.9 PF)	$V_{motor,lim}$	300V

and frequency is the difference between resonance frequency, f_{res}, and motor's electrical frequency, f_r, is varying. The output of DC-link voltage balance controller is V_{sn} in zero sequence (n axis). The voltage, V^r_{dqn}, which is the total sum of the output of three sub-controllers, are synthesized by the inverter.

Although each controller operates as designed in stand-alone mode, integrated controller could fail to accomplish whole control purposes of the three controllers; motor torque and speed control, DC-link voltage balancing, and grid current control for grid code. This happens when the voltage sum is distorted by PWM limiter whose hexagonal range depends on DC-link voltage at the instant of PWM and this may frequently happen due to the high speed operation of IMPSM. To secure all purposes of controllers, the total output voltage, V_{abcn}, which is equivalent to V^r_{dqn} in the rotor reference frame should be remained in PWM voltage range for every PWM instant. That is, available voltage region for motor control should be reduced adequately to keep the total output voltages, V^r_{dqn}, inside of the limiter given by the hexagon boundary. This regulation is performed with reduced maximum available voltage of motor controller, $|V_{dqs,max}|$, related to flux weakening for steady state and an additional limiter named as 'Motor control voltage limiter' whose limited voltage is $v_{cc,lim}$ for consideration of the transient state. The other voltage region is assigned to the other two controllers, and their sharing ratio is determined by k_{damp}. The voltage sharing of three sub-controllers causes trade-off among the controllers, meaning that better performance of a certain controller results in degraded performance of other controllers inherently.

B. Design for steady state voltage sharing

The steady state operation of the system means that motor runs at the rated motor speed and torque, suppressed DC-link voltage difference within a safe operation region of switches, and regulation of grid current satisfying grid code, for example, IEC-61000-3-12 to this system. For the system and controller design, minimum and maximum motor voltage to operate motor at rated torque/speed, $|V_{dqs,max}|_{min}$, and $|V_{dqs,max}|_{max}$, and PF at the moment, allowable voltage difference, and allowable resonance DC-link voltage should be set.

Minimum motor voltage can be derived from the capability curve of IPMSM and inverter based on (4)-(5). The maximum voltage should be inside hexagon. The conventional over-modulation which utilizes corners of hexagon is hard to be applied, because there is no voltage margin for active damping controller near sides and corners of the hexagon. The pulsating DC-link voltage shapes size of hexagon with frequency of 6 times of grid frequency. Hence, maximum voltage should be smaller than average DC-link voltage as (26).

$$\left|V_{dqs,max}\right|_{max} = 1 \cdot \frac{average\ of\ V_{dc}}{\sqrt{3}} = 0.93\frac{V_{dc,peak}}{\sqrt{3}} \quad . \tag{26}$$

Allowable voltage difference, $dV_{dc,max}$ can be calculated as (27), where $V_{sw,max}$ and $V_{sw,min}$ is the larger and the smaller switching voltages at the maximum voltage difference, respectively, and $V_{dc,max}$ is the maximum DC-link voltage. Allowable resonance DC-link voltage, $V_{dc,res,max}$, can be calculated, for example, as (28), where $I_{gridcode,res}$ means permitted grid current at the resonance frequency.

$$\begin{aligned} dV_{DC,max} &= V_{sw,max} - V_{sw,min} \\ &= V_{sw,max} - (V_{dc,max} - V_{sw,max}) = 2V_{sw,max} - V_{dc,max}. \end{aligned} \tag{27}$$

$$V_{dc,res,max} = \sqrt{\frac{L_{g,eq}}{C_{dc}}} I_{gridcode,res} \,. \tag{28}$$

Now let's select desired maximum available motor voltage, $|V_{dqs,max}|$ and k_{damp}. These values should be decided to leave enough voltage margin for the DC-link voltage balancing controller. The sum of output voltage of the motor controller and the active damping controller can be calculated as (29) and (30) with the values in Table 2.

$$\begin{aligned} |V^{r*}_{dqs,damp}| &= |V^{i*}_{dqs,damp}| = |V^{r*}_{dqs} R(\theta_r - \theta_i) + V^{i}_{ds,damp}| \\ &= \left| |V^{r*}_{dqs}| R(\theta_v - \theta_i) + V^{i}_{ds,damp} \right| \approx 298V\,(at\ peak). \end{aligned} \tag{29}$$

$$R(\theta_v - \theta_i) = PF + j\sqrt{1 - PF^2}\,(lagging).$$

$$V^{i}_{ds,damp} = 12k_{damp} = 36V\,(at\ peak)\,. \tag{30}$$

With the MI and PF of this voltage, the worst neutral current at a side of hexagon is calculated as 14A through (8)-(10) and it causes voltage difference to be about 14V at a sampling period as with (7) under the assumption of the balanced grid voltage. This value could shift with duty factors according to the pulsating DC-link voltage, V_{dc}, and voltage difference, dV_{dc}.

For more than several sampling periods (10 periods for this case), voltage difference remains in permitted value and voltage and current vector rotates about 65 degree as (31), reaching next side of hexagon, where neutral current has oppose sign.

$$60° < \frac{(sampling\ periods)Tsamp}{T_{fund}} = 10\frac{360}{20000} = 65° \ . \qquad (31)$$

When $|V_{dqs,max}|$ is larger than minimum DC-link voltage, $|V_{dqs,max}|_{dc,min,}$ due to small capacitance, over-modulatoin of 6 times of grid frequency (360Hz for 60Hz grid) happens regardless of the motor operating frequency. This causes motor current beating along with that frequency even at steady state, and torque (speed), MI, and PF also beat. Additionally, active damping and DC-link voltage balancing controllers' output voltage beat again because their algorithms uses motor MI and PF. This can be avoided by setting $|V_{dqs,max}|$ smaller than the minimum DC-link pulsating voltage.

C. Design for transient state voltage sharing

Unlike to the steady state case, the output of the motor controller would rapidly increase to the outside of $|V_{dqs,max}|$, for example, when load torque changes suddenly. This could cause a malfunctioning of other controllers. To prevent this the 'Motor control voltage limiter' cuts the output and leaves voltage margin to other controllers, especially for DC-link voltage balancing controller. This is because the grid side current regulation is only for steady state. Therefore the limit radius, $V_{motor,lim}$, can be set as $V_{dqs,damp}$ in the steady state, using voltage to the side of hexagon, leaving no voltage to the active damping controller when DC-link voltage is shrunk.

V. Experimental Result and System Design

Fig. 8 Experimental setup

A. Experimental Setup

To verify the stability and performance of proposed controller for the 3-level inverter with small passive elements system, experiment with variety of control parameters has been proceeded. Experimental setup is shown in Fig. 8, whose block diagram, controllers, and their parameters are shown in Fig. 1, 2, 3, 5, and 6, and Table 1 and 2. There are no additional protection circuits at all and a load machine is connected to the IPMSM under test.

B. System purformence with variety of parameters

The control parameters should be chosen properly according to the experimental conditions due to disturbance and distortions such as dead time, actual grid resonance condition, motor harmonics, inductance non-linearity, etc. The efficiency and grid code satisfaction with these small passive elements should be evaluated in the experiments.

Fig. 9 shows grid phase current, DC-link voltage, upper side DC-link voltage, and motor current for several different operating conditions and two different systems. From Fig. 9 (a) it can be seen that the desired performance can be obtained, and (b) shows the performance of 2-level inverter system which has same grid filter but the DC-link electrolytic capacitor is 1.1mF. In Fig 9 (c) the test result with different k_{damp} to (a) are shown. . The Total Harmonic Distortion (THD), Partially Weighted Harmonic Distortion (PWHD), and efficiency of inverter, motor, system are listed in Table 3. The grid code test result of Fig. 9 (a) is in Fig. 10, and shows 5^{th} and 7^{th} due to diode commutation and 11^{th} only with minimum R_{sce} of 316, satisfying grid cord for the system, IEC 61000-3-12. The DC-link voltage of Fig. 9 (a) reveals six pulse and 11^{th} harmonics whose magnitude is about 30V as intended. Maximum DC-link voltage difference is about 50V. Motor current shows 5^{th} and 7^{th} harmonics which originates from motor back EMF harmonics in both inverters. The efficiency of 3-level T-type inverter, (a) case, with grid filter is 97.5%, that of motor is 97%, and total system is 94.5%. The 3-level inverter has better grid current harmonics than 2-level inverter, thank to small filter inductance and active damping controller. 2-level inverter needs more inductance to satisfy grid code. The 3-level inverter efficiency is 1.2% higher comparted to 2-level system while motor efficiency is almost same. This is because decreased motor iron loss due to reduced motor flux compensates the increased motor copper loss as with increased flux weakening current. Fig. 9 (c) shows uncontrolled grid current with unity k_{damp}, failing grid code test due to 11^{th} and 13^{th} harmonic violation. This confirms the analysis of (19)-(23) in III. That is, the test results in Fig. 9 (c) reveal that unity k_{damp} can damp inverter positive feedback only and cannot damp the grid resonance

Fig. 11 shows motor speed, DC-link voltage, upper side DC-link voltage and load torque. Load torque is proportional to square of motor speed and 14N at rated 7200r/min like pump load. During acceleration DC-link voltage and upper side DC-link voltage are regulated as designed. Fig. 12 shows motor speed, DC-link voltage, upper side DC-link voltage and torque reference. The half rated load torque is applied with a slope of 4 pu/s. It can be seen that the speed deviation is less than 200r/min and DC-link voltage and upper side DC-link voltage are regulated as designed.

Table 3. Experimental results with variety of systems

System	THD/PWHD [%]	Efficiency [%] (inv./motor/sys.)
3-level	31.4 / 43.7	97.4 / 97.0 / 94.5
2-level, f_{sw}=8kHz	43.0/48.9(Fail)	96.2 / 97.1 / 93.3
3-level, k_{damp} = 1	41.0/41.7(Fail)	97.2 / 97.0 / 94.2

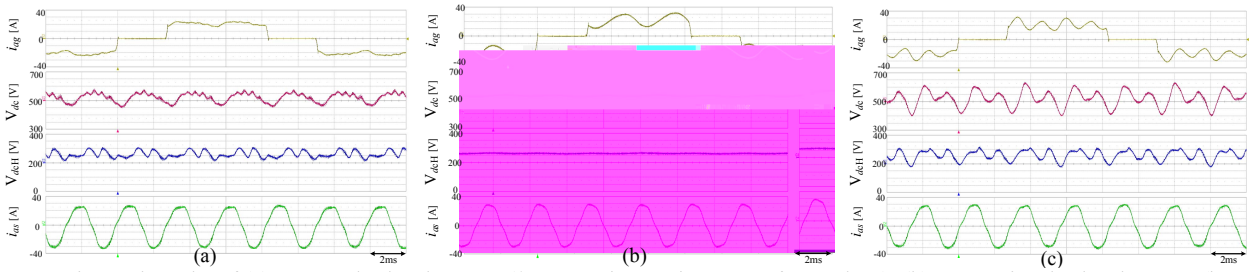

Fig. 9. Experimental results of (a) proposed 3-level system (k_{damp} = 3, $|V_{dqs,max}|$ = 270V, f_{sw} = 16kHz), (b) conventional 2-level system ($|V_{dqs,max}|$ = 300V, f_{sw} = 8kHz), (c) proposed 3-level system (k_{damp} = 1, $|V_{dqs,max}|$ = 270V, f_{sw} = 16kHz).

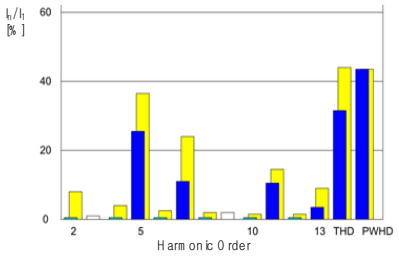

Fig. 10. Test result of grid code satisfaction (Pass; R_{sce} = 316) of 3-level system (k_{damp} = 3, $|V_{dqs,max}|$ = 270V, f_{sw} = 16kHz)

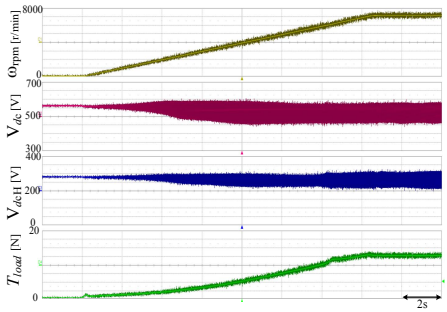

Fig. 11. Experimental result of speed control with pump load.

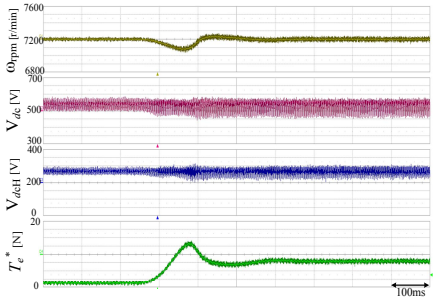

Fig. 12. Experimental result of speed control with load torque variation.

VI. Conclusion

This paper introduced an integrated control method for the 3-level inverter for high speed motor drive with small passive elements, i.e., a small grid filter inductance and DC-link capacitance. The controller has three sub-controllers; motor speed and torque controller, DC-link voltage balancing controller, and active damping controller. These controllers were designed to operate with the small passive elements and the interference between controllers under the limited PWM output voltage was handled through careful controller integration. The analysis and design for sub-controller and overall integrated controller were included and the extensive experimental results with variety of control parameters and systems verified the stability and reasonable performance at both steady state and transient state. This system would improve system efficiency by 1.2% and reduce size and weight of grid filter, DC-link capacitor, and cooling system keeping grid code, compared to 2-level bulk inverter.

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