Harmonic Currents Control of Three-phase Four-wire Grid-connected PWM Inverter Based on High-Order Repetitive Controller

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***Abstract*—In this paper, a repetitive controller with the multi-rate system has been proposed to reduce harmonic currents from a grid-connected PWM boost converter with an LCL filter. The multi-rate system, where different sampling frequency coexists, makes it possible to reduce memory space requirement and computational burden of the repetitive controller. By exploiting the limited current regulation bandwidth due to the resonance of LCL filter, the signal for the repetitive controller can be decimated without any loss. By using decimation and interpolation, the memory space to keep the signals can be reduced conspicuously. In this paper, a technique reducing memory space and computational burden has been proposed and it was verified through a computer simulation and an experimental test. The experimental results show that there is no performance difference between conventional system and the system with the proposed technique. While, through the proposed technique, the memory space and the computational burden has been reduced by 64% and by 41%, respectively.**

***Index Terms*—repetitive control, multi-rate system, harmonic currents control, grid-connected PWM inverter**

I. Introduction

The repetitive controller is a powerful tool to handle periodic disturbance in mechanical rotary system and power system. Applications of repetitive controller involves microscopes [1], disk driver [2], UPS [3], active filter [4], and etc. The repetitive controller is mathematically equivalent to parallel operation of infinite number of resonant controllers [5] and has advantages such as a simple structure and comparable disturbance rejection capability to resonant controllers. However, as a type of learning controller, the repetitive controller has disadvantages such as slow response and large memory space [6]. Especially, High Order Repetitive Controller (HORC) requires more memory space than the general repetitive controller. HORC can be constructed for diverse purposes, for example, frequency robustness HORC and noise robustness HORC [7]. These HORCs have better performance when the higher order it has, but as the order of HORC is getting higher, the memory space is also getting larger.

To overcome this demerit of HORC, an odd-harmonic order repetitive controller is proposed in [6]. Since three-phase three-wire grid-connected system has no even-harmonic components, by removing control capability of even-harmonic components, the memory space of the repetitive controller can be reduced by half and the dynamics of the controller had been improved. With a similar approach, $6k \pm 1$ harmonic repetitive controller had been proposed in [8]. This controller could have smaller memory space and faster dynamic performance by further limiting control capability exploiting the characteristics of three phase balanced system.

In this paper, it is proposed that a repetitive controller can be improved by applying multi-rate system, where signal decimation could be used. The controller based on multi-rate sampling can save the memory space conspicuously and may have less computational burden while keeping the same disturbance rejection performance. Proposed multi rate system has been applied to a grid-connected four wire PWM boost converter with LCL filter where the bandwidth of the signal has been inherently limited because of the resonance of LCL filter. Detailed design procedures are provided for the implementation of the proposed repetitive controller in a multi-rate system and it is verified using simulations and experimental results obtained with a 5kW grid-connected PWM converter for Battery Energy Storage System (BESS) using DSP-based digital control system.

II. Principle of Repetitive Control with Multi-rate System in Grid-Connected Inverter with LCL Filter

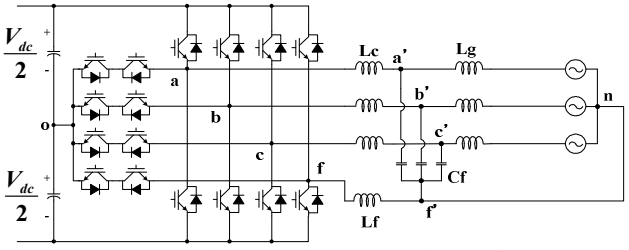


Fig. 1. Grid connected converter with LCL filter

Repetitive controller should have a low-pass filter to keep the stability at high frequency region [6]. And this filter plays a role as limiting the controller's bandwidth. LCL filter also limits its bandwidth inherently. In the case

of grid connected converter with LCL filter as shown in Fig. 1, the bandwidth of the controller should be limited to a half of the resonant frequency of LCL filter for the stability of the current controller considering the signal delay and control margin. In this case, the bandwidth of the signal for the repetitive control would be 1/6~1/8 times of the switching frequency because the resonant frequency of LCL filter is designed below 1/3~1/4 times of PWM switching frequency in general [9].

In the double-sampling system which is used for the extension of the control bandwidth of current regulator up to one tenth of the switching frequency [10], the Nyquist frequency is equal to the switching frequency. In that case, the bandwidth of the signal for the repetitive control would be at least one eighth of the Nyquist frequency [9, 11]. It means that one eighth times of system sampling frequency is enough for signal storage and recovery.

Considering the principles of the repetitive control that signal of one period of the fundamental wave should be stored in the repetitive controller, the band-limited signal can be saved in much slower sampling rate, where the signal can be stored in much smaller memory space. Then, the memory size of repetitive controller can be conspicuously saved if there is a large difference between control band-width and sampling frequency like this control system where the signal of the grid-connected converter is sampled and controlled at twice of the switching frequency. The signal saved in the slower sampling rate can be easily reconstructed without any loss of the information using expander and interpolation filter, which will be explained in chapter 3 in this paper.

Accordingly, this paper presents the complete design methodology for the harmonics current control scheme. By using 2nd order HORC having two sampling rate system, the control system can have robustness for frequency variation but also less memory space compared to general HORC. Especially, it employs a poly-phase representation to reduce the number of multiplication per unit time for FIR filter. Harmonic currents controller is implemented over the L filter under the assumption that LCL filter can be approximated to L filter. This assumption would be justified if the control bandwidth of the current regulator is far less than resonant frequency of LCL filter. The proposed repetitive controller with multi-rate system also can be applied to other types of repetitive controller like aforementioned odd-harmonic order repetitive controller [6] or $6k \pm 1$ harmonic repetitive controller [8].

III. Design of High Order Repetitive Controller with Multi-rate System

In this study a plug-in repetitive controller is used for the harmonic current control of LCL filter system by which the repetitive controller can be added to existing controllers like PI controller [12]. Thus it is easy to design the repetitive controller since the existing controller can be used and the repetitive controller works as an auxiliary harmonic regulator.

A. Design of High Order Repetitive Controller for Harmonic Current Control

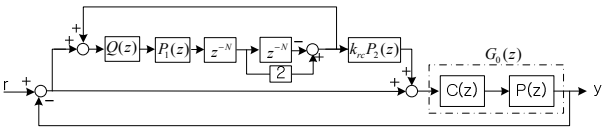


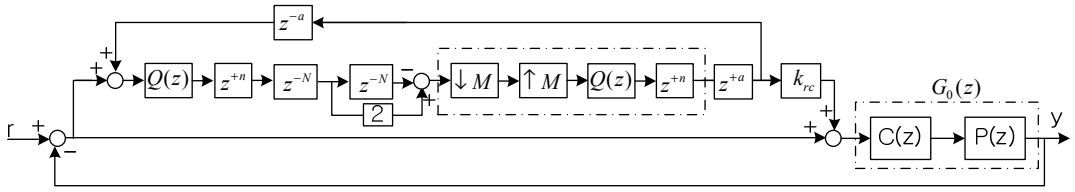
Fig. 2. Detailed plug-in High Order Repetitive Controller in d-q-n reference coordinate

Fig. 2 is a block diagram of a typical plug-in 2nd high order repetitive controller. In this figure, z^{-N} is time delay function for period of the fundamental frequency. Q(z) is '2n' order Finite Impulse Response (FIR) low-pass filter for limiting bandwidth. $P_1(z)$ is a compensator for the phase delay of FIR filter implemented by z^{+n}. $P_2(z)$ is stability compensator for the phase delay of total system implemented by z^{+a}. C(z) and P(z) is PI current regulator and transfer function of LCL filter in synchronous d-q-n reference coordinate, respectively.

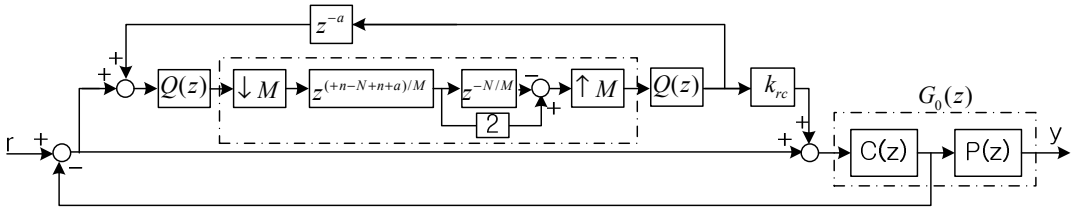
As the LCL filter has a resonant point and the controller may excite this resonance, cut-off frequency of Q is set below the resonant frequency but above maximum harmonic frequency to be eliminated. To extent controller's bandwidth as much as possible without resonant, a higher order FIR filter can be used to reduce transition region in the filter characteristics at the cost of heavier computational burden. On the other hands, a lower order FIR filter may reduce the computational burden while the bandwidth would be shrunken. Shortly, there is a trade-off relationship between filter's order (computational burden) and the bandwidth of the controller.

Band-limited signal by Q filter is stored in N memory space (z^{-N}) and reused for next fundamental period repetitively. In this system, the number of required memory space is (2N-n) + (2n+1) where 2N-n is from z^{-2N+n}, "2n+1" is from the Q filter.

If the repetitive controller and the PI controller have limited bandwidth below the resonant frequency, the LCL filter can be approximated as an L filter. And accordingly, $P_2(z)$ can be designed.



(a)



(b)

Fig. 3. Proposed 2nd HORC with multi-rate system block diagram

B. Multi-rate System for Repetitive Controller

As the signal for the repetitive controller is band-limited by the Q filter, the sampling rate for the repetitive controller can be reduced conspicuously. A lower sampling rate system is inserted into the plug-in repetitive control system in Fig. 2. A multi-rate system having two sampling rate (original one and its 1/M sampling frequency) is depicted in Fig. 3.(a). M is determined by the ratio of repetitive controller's bandwidth and the sampling frequency. M can be 6~8 at double sampling system, 3~4 at the single sampling system in the case of a grid connected PWM boost converter system with LCL filter.

As the bandwidth of the signal is already limited by the Q filter, like role of a decimator filter, a decimator and an expander are inserted for construction of multi-rate system. One additional interpolation filter following the expander is also needed for elimination of the image of signal generated by the expander in frequency domain. And, the same Q filter can be used as an interpolation filter [13]. This filter actually acts for filling the zero values introduced by expander, through the interpolation in time domain.

Since the signal passes through two same Q filters, overall pass-band tolerance region of two filters looks like 2 times larger than that of one Q filter. Thus the decimation and interpolation filters with a half of 'pass-band tolerance region' can be used in the proposed multi-rate system while keeping the same harmonic regulation performance.

The system in Fig. 3(a) can be rearranged as the system in Fig.3 (b) by using the noble identities of multi-rate systems [13]. From Fig. 3, it can be seen that the number of required memory space in multi-rate system decreases from (2N-n)+(2n+1) to (2N-2n-a)/M+(4n+2+a). As M is getting larger, the less memory space is needed. It is worth to note that (2N-2n-a)/M should be an integer number.

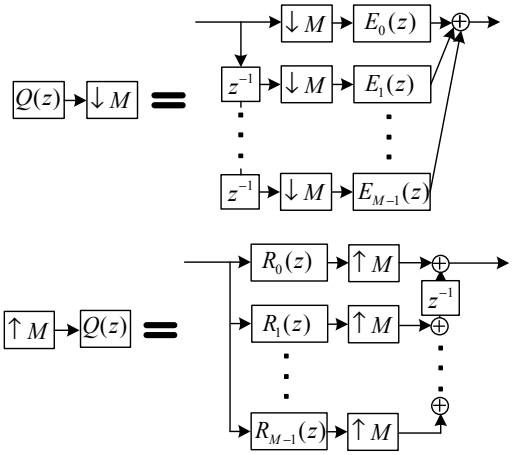


Fig. 4. Poly-phase implementations of a decimation filter and an interpolation filter for Q filter in multi-rate system.

Q(z) designed by FIR filter can be represented as (1) , which is called Poly-phase representation, and its implementation in multi-rate system is shown in Fig. 4. The poly-phase representation permits computational efficiency in use of decimation or interpolation filter [13]. This method can't reduce the total number of multiplication but enables faster calculation by decreasing the number of multiplication per unit time in real-time operating systems.

$$\mathrm{Q}(z) = \sum_{n=-\infty}^{\infty} q(n)\, z^{-n} = \sum_{l=0}^{M-1} z^{-l} E_l(z^M) = \sum_{l=0}^{M-1} z^{-(M-1-l)} R_l(z^M)$$

$$\text{where,} \quad \left\{ \begin{array}{c} E_l(z) = \sum_{n=-\infty}^{\infty} q(Mn+l)\, z^{-n} \\ R_l(z) = E_{M-1-l}(z) \end{array} \right\}. \tag{1}$$

Therefore, from Fig. 4, it can be seen that the number of multiplication per unit time is reduced to 1/M times in the multi-rate system. As a result, the execution time of the decimation and interpolation filter of the multi-rate system may be reduced to 1/M of that of the single-rate

system. Considering an additional interpolation filter, the total execution time of all filters of multi-rate sampling system would be 2/M compared to that of the single sampling rate system.

In short, by applying multi-rate system having M times slower sampling frequency to the repetitive controller, total memory space would be reduced to near 1/M and the execution time 2/M of the single sampling rate system.

C. Simulation for HORC with multi-rate system

To compare the performance of general HORC and HORC with multi-rate system, computer simulation is conducted.

Grid-connected converter with LCL filter for 3-phase 4-wire system as shown in Fig. 1 is used for the simulation. Parameters of the system are listed in Table I. To generate harmonic currents that cannot be suppressed by a conventional PI current regulator, 1~21 order harmonic voltages which has 0.3% of nominal grid voltage magnitude are injected into the grid.

Simulation has been carried out with the MATLAB simulink and PLECS.

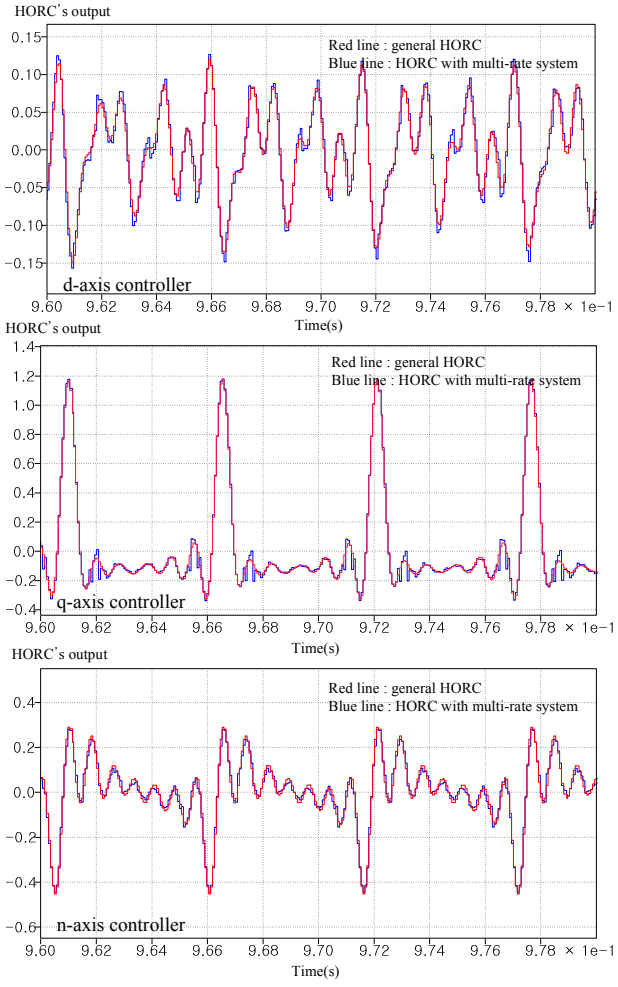


Fig. 5. Comparisons of HORC's output with single-rate system and multi-rate system in d, q, n axis in computer simulation

Fig. 5 and Fig. 6 show repetitive controller's output and the current error in d, q, n axis by using HORC and HORC with multi-rate system(M=4) respectively. In Fig. 5 it can be seen that there is no difference between controller's output of general HORC and that of HORC with multi-rate system.

TABLE I
SYSTEM PARAMETERS VALUES USED IN SIMULATION AND EXPERIMENTS

Description	Symbol	Value
Converter-side inductance	L_c	1.2mH
Grid-side inductance	L_g	0.731mH
Converter-side f-phase inductance	L_f	1.2mH
Filter capacitance	C_f	9uF
DC-link voltage	V_{dc}	384V
Grid voltage(line-line)		220Vrms
Switching frequency		7.2kHz

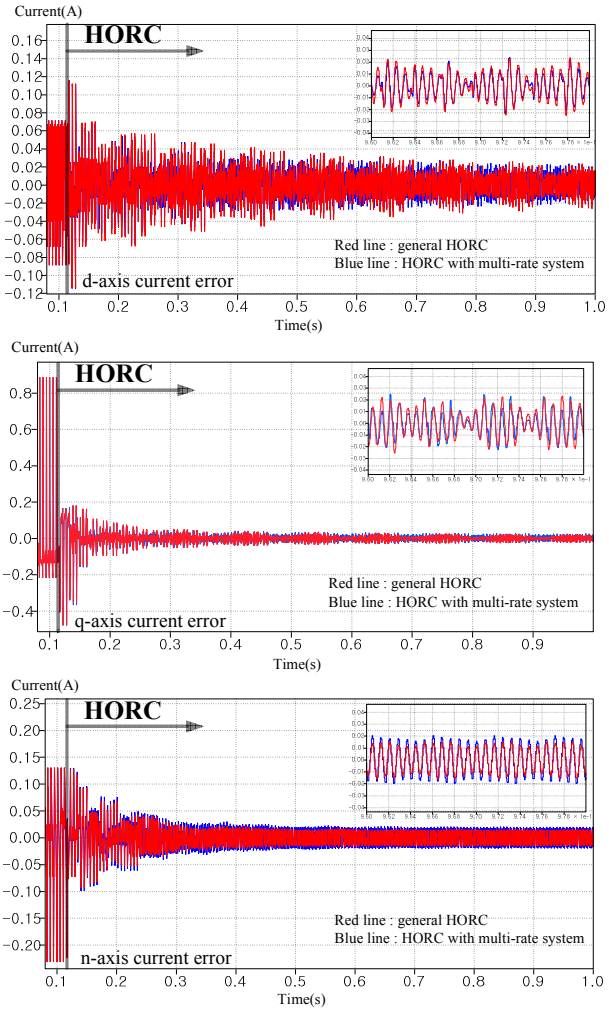


Fig. 6. Comparisons of current error with single-rate system and multi-rate system in d, q, n axis in computer simulation. Zoomed plot is presented in right upper corner

Fig. 6 shows current error in d, q, n axis by using general HORC and HORC with multi-rate system. It is shown that two controllers have the same performance for harmonic current control.

IV. EXPERIMENTS

The parameters of experimental system are the same to the parameters used in the simulation listed in Table I. From the values of LCL filter, it can be derived that the resonant frequency of d, q, axis is $f_{res\,d,q} = 2.490kHz$, and that of n axis is $f_{res\,n} = 2.106kHz$.

To make 'N' as an integer for 60Hz fundamental frequency, the switching frequency has been set as 7.2 kHz. The Q filter is designed with 1.08 kHz pass band edge (up to 19-th harmonic current of fundamental frequency) and stop band edge 1.8 kHz to prevent the excitation of the resonant point of the d, q, n axis LCL filter. The order of FIR filter for the single sampling rate system is 26, and 31 for the multi-rate system.

Table II summarizes the number of multiplications and memory space comparing the conventional (single-rate) approach to multi-rate (M=4) approach for 2nd order HORC. There is 64% reduction of memory space for HORC and the number of multiplication per unit time is decreased by 41% with M=4.

TABLE II
NUMBER OF MEMORY SPACE AND MULTIPLICATION PER UNIT TIME FOR SINGLE AND MULTI-RATE SYSTEM IN D,Q,N AXIS.

	High Order Repetitive Controller (2nd order)	
	Number of Mul. /unit time	Number of Memory
Single-rate system	27×3	494×3
Multi-rate system (M=4)	16×3	180×3
Reduction ratio	41%	64%

Experimental setup is composed of a 3-level 4 leg inverter (rated current: $19A_{peak}$), a lithium-ion battery bank as a DC source, and TMS28346 DSP system for the controller implementation. Three-phase line-to-line $220V_{rms}$, 60Hz, grid is used for experimentation. The experimental test is carried out in the rated condition.

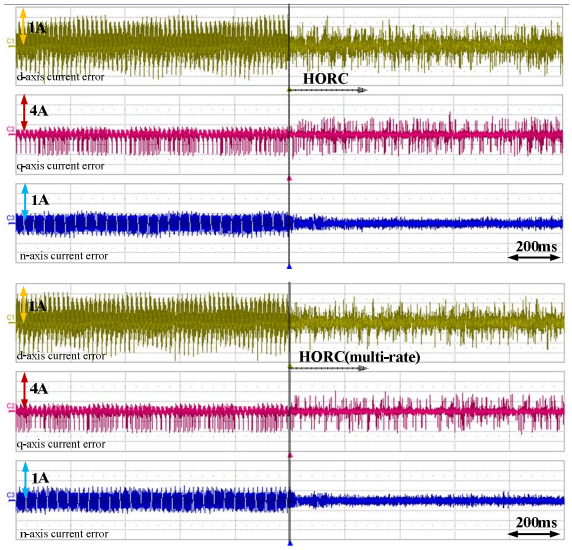


Fig. 7. Comparisons of current error with single-rate system and multi-rate system in d, q, n axis (upper: general HORC, lower: HORC with multi-rate system)

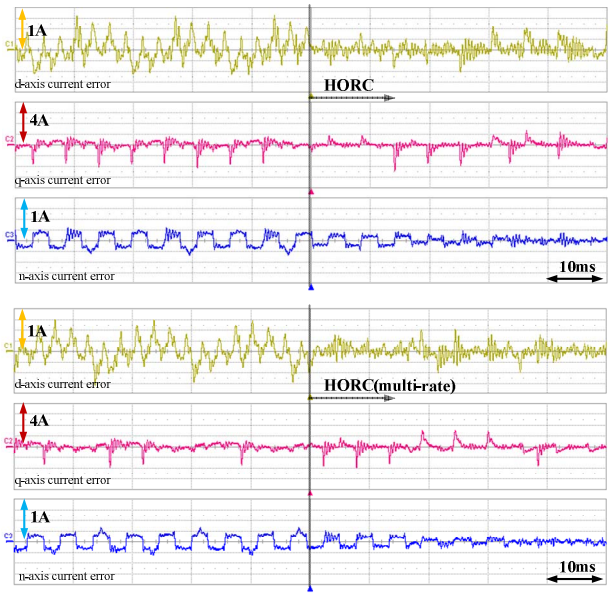


Fig. 8. Zoomed view of Fig.7 (upper: general HORC, lower: HORC with multi-rate system)

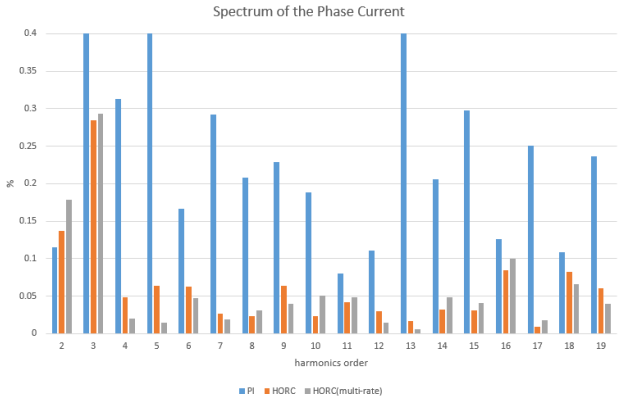


Fig. 9. Spectrum of the A-Phase Current (x-axis: harmonics order, y-axis: % of each component compared to fundamental component magnitude)

Experimental results are depicted in Fig. 7 and Fig. 8 where current error in d, q, n axis with no repetitive controller (only by PI current regulator with 400Hz current regulation bandwidth), general HORC, and multi-rate HORC are shown. Fig. 8 shows the zoomed waveforms corresponding to Fig. 7. The dynamic performances of general HORC and multi-rate HORC are almost identical as shown in Fig. 8.

Fig. 9 shows frequency spectrums of A-phase current using HORC and HORC with multi-rate system. It is shown that there are very similar harmonic spectrums between single-rate HORC and multi-rate HORC.

As shown in Fig. 10, THD of A phase grid current only with the PI regulator is about 2.1%. THD with general HORC is 0.7% and that with multi-rate HORC is 0.8%, and the difference is within measurement tolerance.

The experimental results shown in Fig. 7, 9, 10 reveal almost equivalent performance in steady state operation with general HORC and with multi-rate HORC.

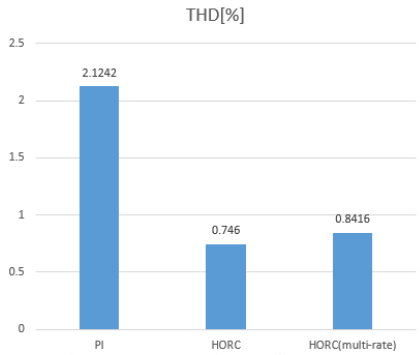


Fig. 10. Comparisons of THD (%)

From all the simulation and experimental results, it can be said that regardless of the conspicuous reduction of memory space and computational burden the performances of the multi-rate HORC are the same with the conventional general HORC.

V. Conclusions

It had been well known that the repetitive controller, a type of learning controller, can effectively reject repetitive disturbances. However, it has disadvantage of large memory space to store the signals to the controller. Especially, more memory space is demanded in the case of HORC. Therefore, repetitive controller is used restrictively or sometimes may demand additional memory bank.

To overcome this demerit, a repetitive controller with multi-rate system has been proposed. In multi-rate system, the number of required memory space can be decreased from "(2N-n)+(2n+1)" to "(2N-2n-a)/M+(4n+2+a)". And the number of Multiplications per unit time also be decreased from (2n+1) to 2(2n+1)/M. In the case of grid connected PWM boost converter with LCL filter, the current regulation bandwidth is much lower than the sampling rate because of the resonance of the filter. In this case by introducing decimation and interpolation techniques, the memory size of the repetitive controller can be reduced conspicuously while keeping the same harmonic regulation performance. Through the computer simulation and experimental results, it is shown that the proposed system can save the memory space and computational burden while keeping the same THD in the grid current. From the experimental results, it has been confirmed that the memory space is reduced by 64% and the computation burden by 41%. .

The proposed system could be applied to odd-harmonic repetitive control [6], $6k \pm 1$ harmonic repetitive control[8] and HORC[7]. In that case, the memory space and computational burden could be reduced further.

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