Anti-Islanding Accelerated by Grid Unbalance Component

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***Abstract*-- In this paper, a method to detect islanding operation of distributed generator (DG) is proposed, which exploits frequency drift accelerated by grid unbalance component, namely negative sequence component of grid voltage. The negative sequence component could be added to the gain of frequency feedback loop in the conventional anti-islanding scheme. To keep the power factor regulation, the displacement power factor (DPF) is considered in the tuning of feedback gain. The PLL (Phase-Locked Loop) with low bandwidth is used to replace the nominal frequency in calculating frequency deviation, and this brings the reduction of unnecessary reactive power injection during normal grid connected operation. The experimental results are shown to verify the effectiveness of the proposed method, which show that both detection time and NDZ (Non-Detection Zone) are improved. Also, the performance of the proposed method with multiple DG systems is discussed by introducing the equivalent single virtual inverter. The simulation and experimental results show validity of discussions.**

***Index Terms*— anti-islanding, frequency drift method, negative sequence voltage acceleration, NDZ of multiple DG.**

I. INTRODUCTION

In the operation of the distributed generator (DG), islanding must be taken into account. The islanding is defined as a condition in which a portion of the utility system, which is energized by one or more local electric power systems through the associated point of common coupling (PCC), is electrically separated from the remainder of utility system [1], [2]. Because islanding can be a threat to the grid operation, anti-islanding is mandatory feature for DGs [1]-[3].

The anti-islanding, which means the method to detect islanding by DGs, can be divided into passive and active methods [4].

In some passive methods, based on monitoring grid parameters, the grid unbalance is significant feature to distinguish islanding. In [5], the negative sequence voltage, current and impedance extracted through wavelet transform were indicator of islanding operation. The voltage unbalance variation was also candidate for monitoring parameters to detect islanding operation [6], [7]. In [8], instead of voltage unbalance, the magnitude of negative sequence was adopted as main indicator.

In the case of active methods, which perturb grid intentionally by inverter and observe reaction of grid parameters, grid unbalance is still interesting features for constructing algorithm. In [9] and [10], the negative sequence current or negative sequence power was injected. After islanding, the voltage imbalance made by injected components was varied enough to detect the islanding operation. The negative sequence voltage was injected through inverters in [11], in order to estimate negative sequence impedance at PCC. The positive feedback between active current and voltage unbalance factor was also suggested [12].

However, in passive anti-islanding, the threshold for voltage unbalance to distinguish islanding operation is ambiguous. In active anti-islanding, there are no considerations for parallel operation. Despite of these drawbacks, the grid unbalance factor is still fascinating parameter to recognize the islanding operation.

The anti-islanding using the positive feedback between reactive power and grid frequency is one of the most popular methods equipped in many grid connected inverters [4], [13]-[17]. For single inverter, the analysis about non-detection zones (NDZs) based on phase criteria [13] or descriptor system technique [14] is suggested and verified. Especially, the operation of parallel connected inverters was also considered by many literatures such as reported in [15] and [16]. Although the positive feedback is well functioning under islanding, the only frequency feedback has limit in reducing detection time.

In this paper, the negative sequence component of grid voltage is used to accelerate frequency drift after islanding. If the load connected after islanding is not perfectly balanced, the negative sequence voltage can be observed, and this can be exploited to accelerate frequency drift.

To keep the power factor regulation, the displacement power factor (DPF) is considered in the turning of the positive feedback gain. In the proposed method, the grid frequency estimated by low bandwidth phase-locked loop (PLL) replaces nominal frequency which informs the frequency deviation. This additional PLL guarantees the minimization of unnecessary steady state reactive power, which is induced by positive feedback gain, during grid connection.

Since the acceleration may be activated by minute grid unbalance, the proposed method has potential to shrink the NDZ of conventional positive feedback anti-islanding as well as to reduce the detection time conspicuously. This possibility of improvement is verified by computer simulation and hardware experimental test.

In this paper, the equivalent virtual single inverter is proposed to analyze the NDZ of multiple DG system. This virtual inverter can emulate the operation of multiple inverters and the NDZ of the multi-DG system can be obtained by analyzing the NDZ of equivalent single inverter. The concept of replacement would be detailed and supported by simulation and experimental results.

II. Proposed Algorithm

A. Acceleration factor

The negative sequence component of grid voltage (NSV) is direct indicator for the grid unbalance. By adding the gain proportional to the NSV into the gain of positive feedback loop, the divergence speed of grid parameter can be accelerated.

Although any anti-islanding based on positive feedback can be modified by the proposed concept, the frequency drift anti-islanding can be the most likely viable candidate. To compare the performance of the frequency drift due to the acceleration factor, the anti-islanding in [17], where the positive feedback is implemented by simple first order polynomial, is selected as a conventional method.

To construct acceleration by grid unbalance, the gain proportional to the NSV is added to the conventional gain in the feedback loop as shown in (1).

$$i_d^* = \left(K_q + K_{Vn}|V_n|\right)(f - f_0)I_s, \tag{1}$$

where K_q is positive feedback gain of conventional frequency drift anti-islanding, $|V_n|$ is magnitude of NSV of grid voltage, K_{Vn} is constant multiplied to NSV. $(f - f_0)$ is frequency deviation and f_0 represents nominal frequency of grid.

As NSV is getting larger after islanding due to the unbalance of load, feedback gain would be boosted and the frequency drift is getting larger, and the islanding detection time would be getting smaller. In addition, due to acceleration using NSV, under condition of unbalanced load, the islanding can be detected which couldn't be distinguished by conventional anti-islanding.

B. Design based on displacement power factor

To design feedback gain, the displacement power factor (DPF) of inverter during normal grid connected operation is considered instead of quality factor of islanding load which is design factor in [17]. In normal operation mode, the grid frequency resides in normal range. However, the frequency deviation causes the reactive power injection because of frequency drift algorithm. Because the DPF is degraded by this reactive power, the feedback gain to maintain DPF within the limited range to keep the power factor regulation such as described on [1] should be considered.

The first feedback gain K_q can be designed to constrain DPF within the limited range in normal frequency range. The gain linked to NSV (K_{Vn}) can be set to constrain DPF even though the NSV occurs during grid connection. The feedback gains, K_q and K_{Vn}, can be set according to (2) and (3) under the consideration of the magnitude of grid voltage and the worst NSV at grid connection.

$$K_q = -\frac{\sqrt{DPF^{-2}-1}}{|\max(f-f_0)|}, \tag{2}$$

$$K_{Vn} = -\frac{\sqrt{DPF^{-2}-1}}{u_v V_{base,pk}|\max(f-f_0)|}, \tag{3}$$

where $V_{base,pk}$ is a nominal peak value of grid phase voltage, u_v, the worst ratio of negative and positive sequence component of voltage at grid connection. In here, base DPF was designed as 0.98.

Because the each feedback gain was designed independently, the reactive power due to the algorithm in the worst case becomes larger than aimed one. As the result, the designed gain may make actual DPF smaller than the required DPF. In this paper, a technique is proposed to overcome this degradation of DPF.

C. Additional PLL with low bandwidth

In (1), to identify the frequency drift, the nominal frequency is used. However, the grid frequency couldn't always be nominal value, but could be a certain value in allowable range. In these conditions, the frequency drift can produce unnecessary reactive power continuously. To minimize reactive power in the steady state, the frequency estimated by PLL with low bandwidth can replace the nominal frequency in calculation of frequency deviation. In steady state, the additional low bandwidth PLL follows the frequency estimated by original PLL and the frequency deviation would be decreased to around zero. After islanding, due to the difference of diverging speed of frequency in each PLL, the positive feedback according to the frequency deviation would be activated. Thanks to the additional low bandwidth PLL, DPF of inverter could be minimized in the steady state and the degradation of DPF due to the independently designed gain could be alleviated.

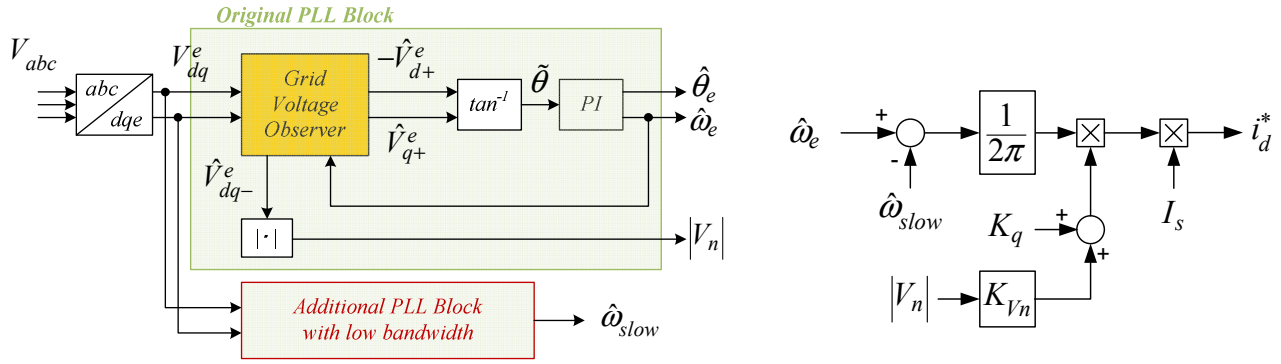


Fig. 1. Control block diagram of the proposed anti-islanding algorithm

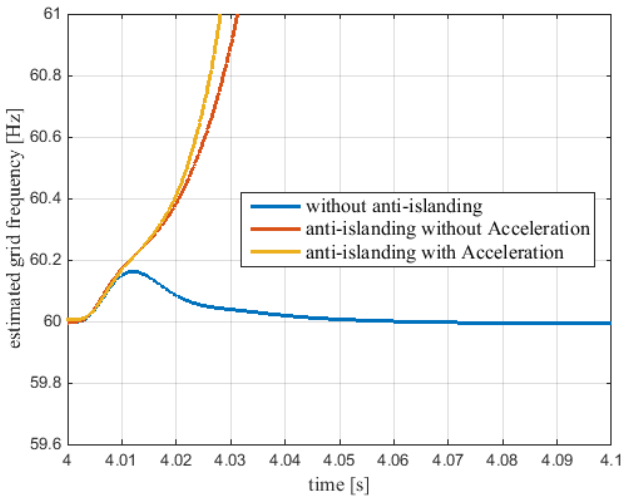


Fig. 2. Islanding simulation – balanced load (Q_f = 2.5)

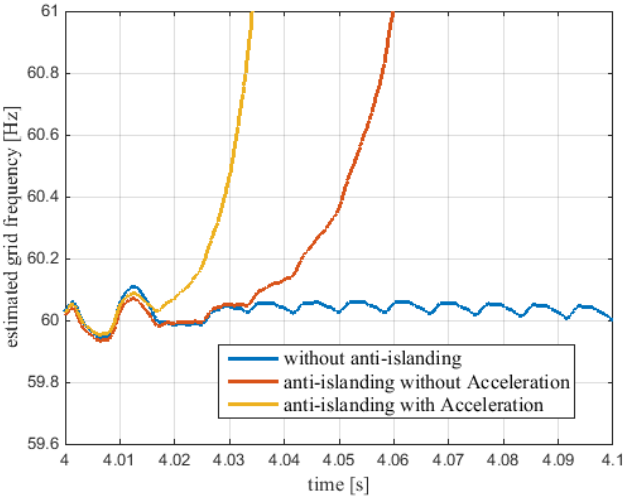


Fig. 3. Islanding simulation – unbalanced load (Type 1)

D. Negative sequence voltage extraction

Some PLL can extract positive sequence voltage naturally [18], [19]. Without using extra block to extract NSV, the NSV can be obtained by subtracting positive sequence voltage from the grid voltage. In this paper, the grid voltage would be estimated by grid voltage observer in [19].

$$\hat{V}_{d-}^{e} = V_{d}^{e} - \hat{V}_{d+}^{e}, \tag{4-a}$$

$$\hat{V}_{q-}^{e} = V_{q}^{e} - \hat{V}_{q+}^{e}, \tag{4-b}$$

$$|V_n| = \sqrt{\hat{V}_{d-}^{e\ 2} + \hat{V}_{q-}^{e\ 2}}, \tag{5}$$

where V_d^e, V_q^e stand for grid voltage, $\hat{V}_{d+}^e$, $\hat{V}_{q+}^e$ are estimated positive sequence components of grid voltage, and $\hat{V}_{d-}^e$, $\hat{V}_{q-}^e$ are estimated negative sequence components of grid voltage. All variables are represented by *d*-*q* component on synchronous reference frame.

In Fig. 1, the overall block diagram of the proposed algorithm is represented.

E. Simulation Results for Single Inverter

With balanced load, such as RLC load descripted in [1]-[3], the grid unbalance couldn't be observed after islanding. The proposed algorithm can't show effectiveness compared to conventional anti-islanding under this load condition. The Fig. 2 shows the islanding test results under load dictated in [1]. The test circuit is set according to [1]-[3]. An islanding is occurred in 4 s. Both anti-islanding can detect islanding condition and the detection time is under 23ms regardless of existence of acceleration. The frequency to trigger over frequency relay is assumed to be 60.5 Hz.

Under unbalanced load condition, the frequency drift was effectively accelerated. In Fig. 3, the test results under unbalanced load condition are shown where the load consists of combination of balanced RLC load, single phase rectified load and three phase rectified load.

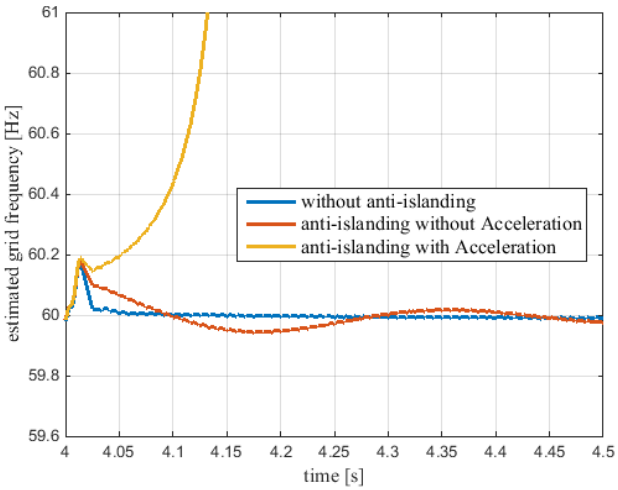


Fig. 4. Islanding simulation – unbalanced load (Type 2)

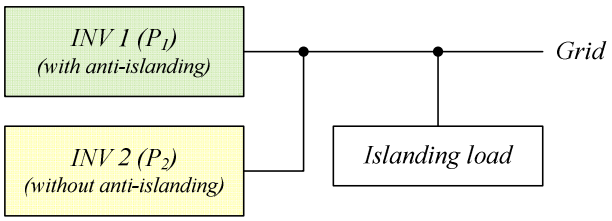
The specific values of load used in simulation are arranged in Table I in Appendix. Without anti-islanding, the inverter couldn't detect abnormal grid situation. With anti-islanding, both algorithms can drift grid frequency and trigger over frequency relay. However, the detection time with acceleration becomes around 30 ms which is faster than that with conventional method (around 53 ms).

III. Discussion for Non Detection Zone

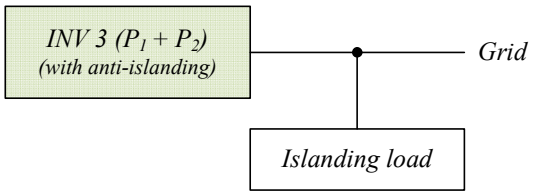
A. Non-detection zone of single inverter

As shown in simulation results, under balanced load condition during islanding, there is no remarkable advantage due to the proposed algorithm. The NDZ is similar to the conventional one and could be represented by load map in [13] or [14].

However, compared to the NDZ of conventional method, the NDZ of the proposed method can be reduced under unbalanced load condition. The simulation results in Fig. 4 with another unbalanced load case clearly demonstrate the effectiveness of the proposed algorithm. Although the conventional drift method couldn't detect



(a) Two parallel inverters



(b) Single virtual inverter

Fig. 5. Equivalent systems to analyze NDZ

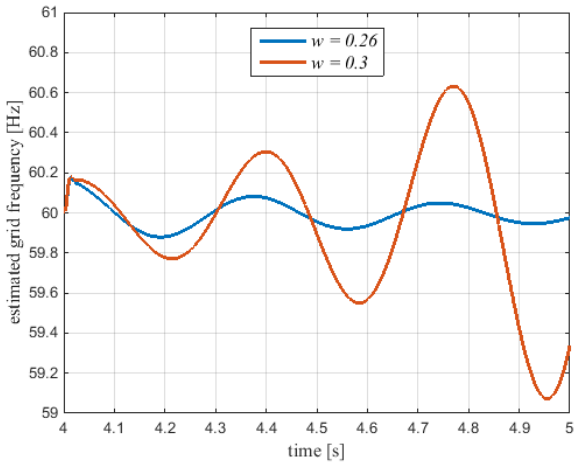


Fig. 6. Single virtual inverter case - Balanced load (Q_f = 2.5)

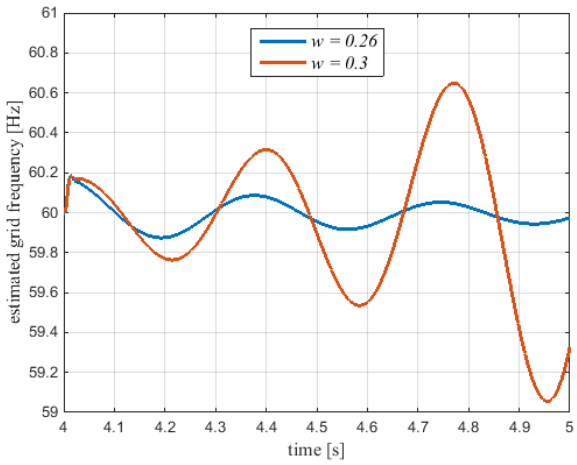


Fig. 7. Two parallel inverter case - Balanced load (Q_f = 2.5)

islanding due to the convergence of grid frequency, the anti-islanding with the NSV acceleration could drift frequency over normal range where the OUF (Over/Under Frequency) relay could be triggered. This result shows that the proposed method has potential to shrink the NDZ of conventional positive feedback anti-islanding conspicuously.

B. Non-detection zone for multiple DG system

If several inverters of multiple DG systems, which use the same frequency drift method for the anti-islanding are connected in parallel, the whole system would show the characteristics as single inverter with the algorithm. The NDZ of this multi-inverters system can be analyzed according to [13] or [14]. In [15] and [16], the analysis of NDZ on two inverter case is discussed. However, it is hard to extend the result to arbitrary number of inverters.

In the case of proposed method including conventional frequency drift anti-islanding, by handling the multi-inverter system as single inverter, the phase criterion or descriptor system technique also can be easily applied to analyze NDZ for the multi-inverter system. At first, a model with two inverters in Fig. 5 (a) can be considered. The inverter with the proposed algorithm (INV 1) operates with another inverter without any frequency drift algorithm including reactive current injection (INV 2). The capacity ratio of INV 1 to total system is designated as w. Second, the single virtual inverter (INV 3) which has the same power capacity as the sum of INV 1 and INV 2 can be considered as shown in Fig. 5 (b) and the operation of whole system seems the same to operation of this single virtual inverter. The INV 3 acts like a single inverter having feedback gain which is equivalent to the product of feedback gain of INV 1 and the capacity ratio of INV 1 to INV 3. The feedback gain of INV 3 can be thought as,

$$i_d^* = w\left(K_q + K_{Vn}|V_n|\right)(f - f_0)I_s. \tag{6}$$

To verify the effectiveness of the proposed equivalent single virtual inverter concept, two cases are simulated. In the first case, two inverters (INV 1 and 2) are operated in parallel. The only one inverter (INV 1) is equipped with the proposed islanding detection method and the capacity ratio is manipulated. In the other case, a single inverter (INV 3) is operated and its feedback gain is set under the consideration of the capacity ratio.

To get positive feedback gain, DPF was designed as 0.98 and the quality factor of the islanding load is set as 2.5. Using equation in [17] and calculating reversely, it is revealed that the minimum capacity ratio, w_{min}, to detect islanding was about 28% for single inverter and it is confirmed through the simulation. In Fig. 6, the simulation results are shown, where the capacity ratio has been set as 0.3 and 0.26 and a single virtual inverter is operated. The w over 0.28 makes frequency diverge in islanding and may trigger OUF relay. On the other hand, the w under 0.28 couldn't detect islanding due to the convergence of grid frequency.

In Fig. 7, two inverters are operated in parallel and islanding detection capability is tested. Also, the capacity ratio of INV 1 has been set as 0.3 and 0.26. The results show that the frequency drift of parallel inverter is same to that of INV 3. That is, the inverters operating in parallel can be replaced by single virtual inverter of which capacity is same to the whole system and the NDZ of parallel inverter can be obtained through this single inverter. In this discussion, the dynamics of PLL in each inverter are assumed to be the same.

Even in unbalanced load, analogy between parallel inverters and an equivalent single inverter would be valid. The Fig. 8 and 9 shows the results of islanding for equivalent single inverter and two parallel inverters. The tendency of frequency drift after islanding of two parallel inverters is matching to that for single inverter. The capacity ratio has been set as 0.2. In both case, the conventional anti-islanding couldn't operate well. By applying the proposed acceleration method, the islanding may be detected and this means that the NDZ has been reduced.

This concept would be able to extend to the arbitrary number of multi-inverters. If each inverter has different capacity, the feedback gain of equivalent single inverter, where the capacity is the same with whole system, is decided by adding the gain of each inverter multiplied by weighting factor, w_i, meaning each inverter's relative power to the whole system. The injected current of the equivalent single inverter representing whole system can be deduced as (8). The positive feedback gain of inverters which have no islanding detection method would be set to zero.

$$w_i = \frac{P_i}{P_{tot}}, \tag{7}$$

$$\begin{aligned} i^*_{d,eq} &= (f - f_0) \sum_i (K_{q,i} + K_{Vn,i}) I_{s,i} \\ &= (f - f_0) \sum_i w_i (K_{q,i} + K_{Vn,i}) I_s, \end{aligned} \tag{8}$$

where 'i' represents index of each inverter, P_i is power of each inverters and P_{tot} is total power of whole system.

In Fig. 10, an equivalent single inverter representing multiple DG system is depicted. By handling this virtual inverter, the NDZ of multiple inverters could be specified by conventional analysis based on phase criterion in [13] or state-space analysis in [14].

IV. Experimental Results

To verify the performance of proposed algorithm and the discussion about NDZ, islanding test with the hardware experimental setup is carried out. The circuit which is commonly specified in international standards such as [1]-[3] is constructed. The parameters of grid and load, and controllers for experimental test are arranged on Table II in Appendix. The positive feedback gains are designed based on (2) and (3). Due to the manufacturing tolerance, the islanding load, which consists of three phase parallel RLC, has quality factor as 2, 59.6 Hz as the resonant frequency, and 3% of unbalance.

In Fig. 11, the experimental results of the case of single inverter are shown. Without anti-islanding, in Fig. 11 (a), the frequency estimated by the original PLL is drift and the additional PLL's frequency is followed after islanding. However, since the frequency is converged and the operation frequency is in normal range, which is set as 58 to 62 Hz in this experiment, the islanding couldn't be detected and the inverter feeds power continuously to the load. The negative sequence voltage becomes about 3% of rated voltage after islanding, which means the existence of unbalance in islanding load.

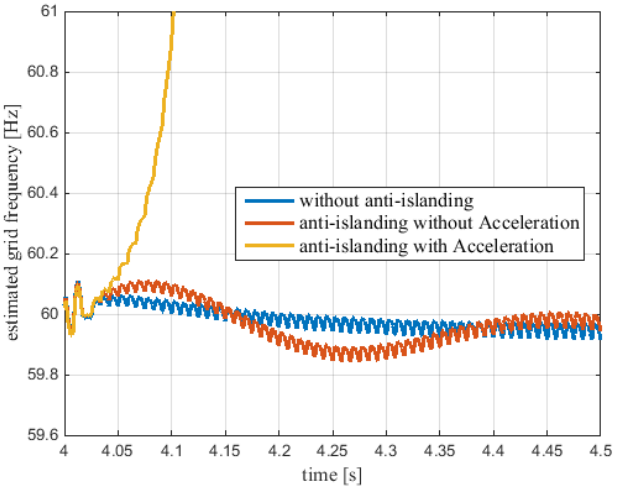


Fig. 8. Single virtual inverter case - Unbalanced load (Type 1)

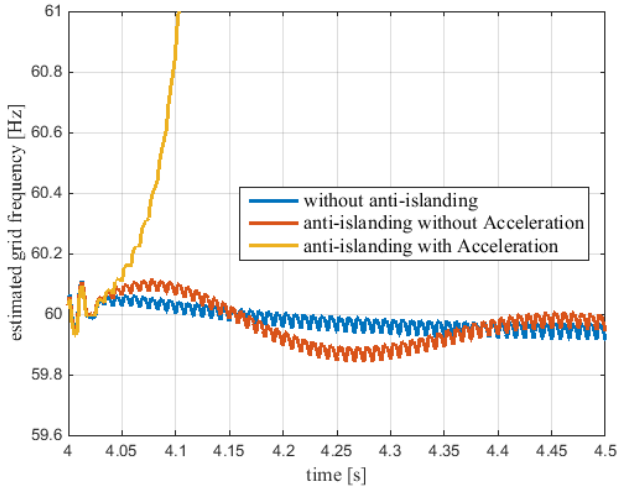
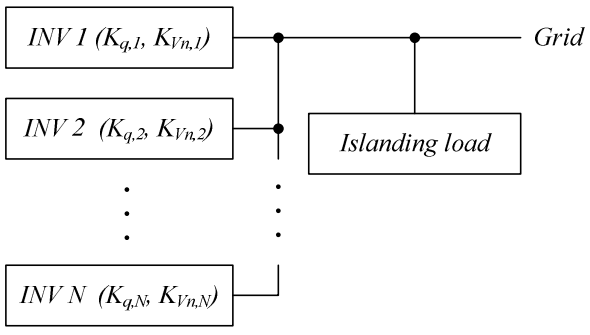
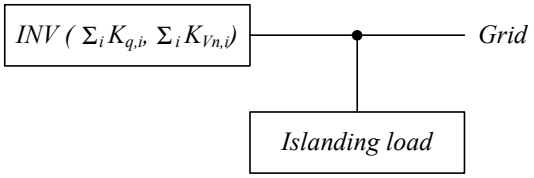


Fig. 9. Two parallel inverter case - Unbalanced load (Type 1)

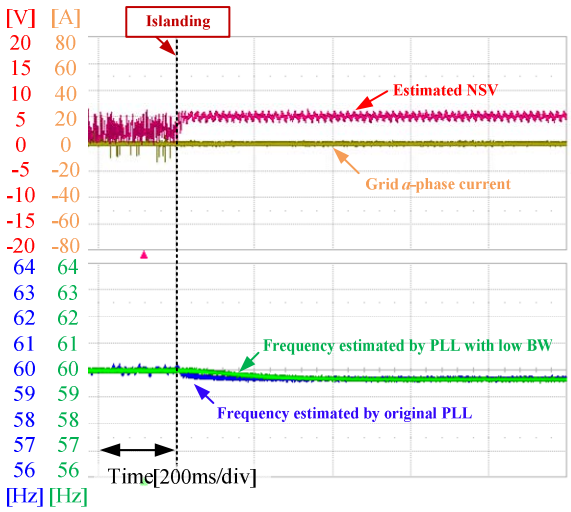


(a) Multiple inverters

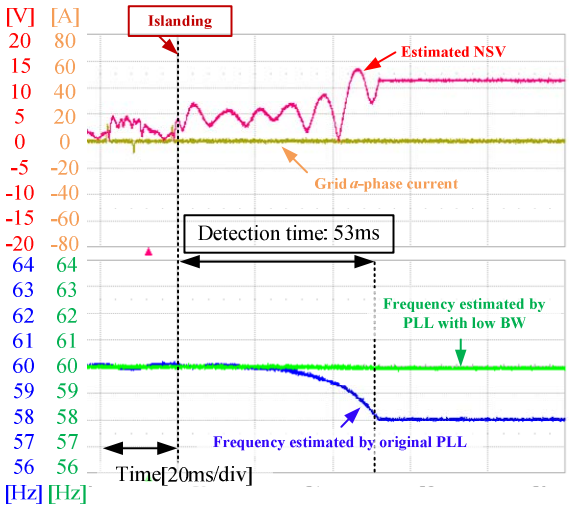


(b) Equivalent single inverters

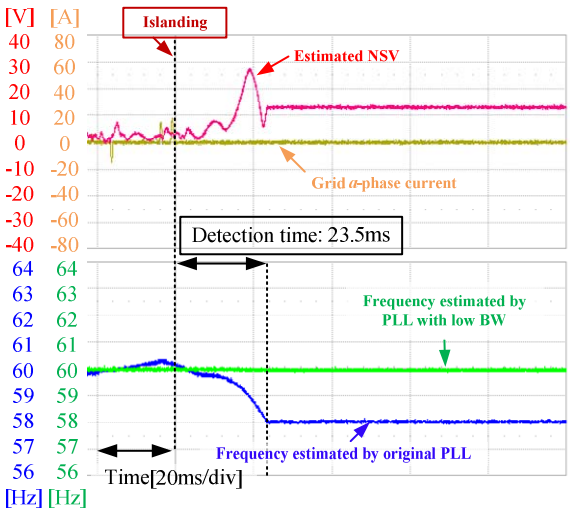
Fig. 10. Equivalent systems to analyze NDZ



(a) Without anti-islanding



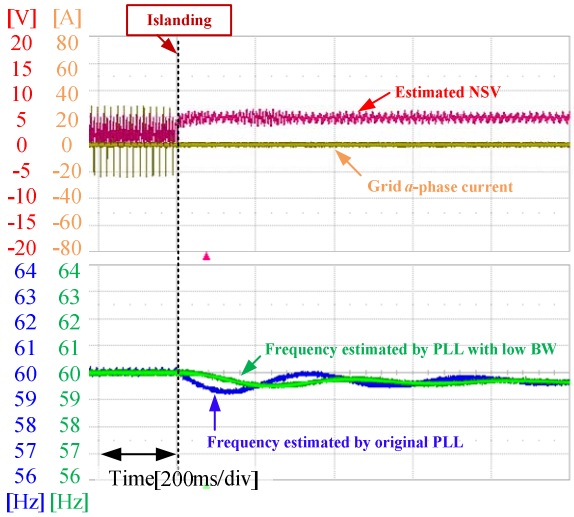
(b) Conventional anti-islanding



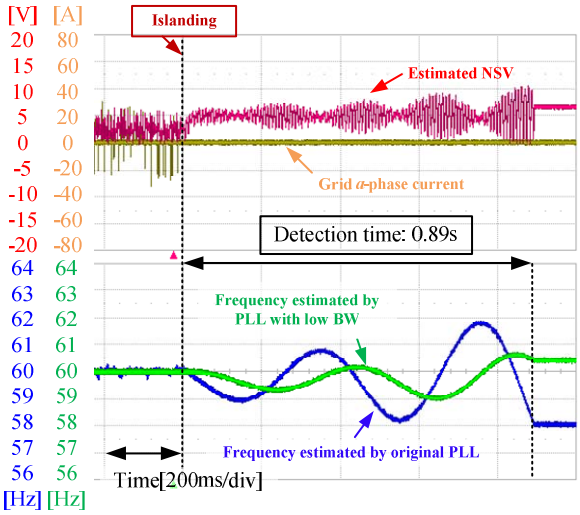
(c) Anti-islanding with acceleration

Fig. 11. Experimental results – single inverter

In Fig. 11 (b) and (c), both anti-islanding algorithms can drift frequency to abnormal range. While the case using only K_q reveals 53ms as the detection time, that using both K_q and K_{Vn} reveals 23.5ms. Even though



(a) $w = 0.2$



(b) $w = 0.25$

Fig. 12. Experimental results – single inverter

estimated NSV after islanding is around 3% of rated voltage which is induced by unintentional small unbalance in the load, the conspicuous enhancement of the islanding detection time has been demonstrated. Observing the experimental results, the dynamics of the frequency in additional PLL in islanding was much slower than the original's one after islanding. The frequency of additional PLL would not degrade the positive feedback in islanding as well as would obtain the rejection of unnecessary reactive power injection in steady state with normal grid connected operation.

For islanding load with quality factor 2, the minimum capacity ratio to detect islanding was about 23% for single inverter, which can be deduced from result on the section III, and this value could become border line of the NDZ of conventional anti-islanding algorithm. In Fig. 12, the islanding test results for single inverter equipped with only conventional anti-islanding with capacity ratio 0.2 and 0.25 are depicted. The inverter with smaller capacity ratio than threshold value couldn't drift frequency at PCC, and OUF relay has not been triggered. In the case of larger capacity ratio, the grid frequency after islanding

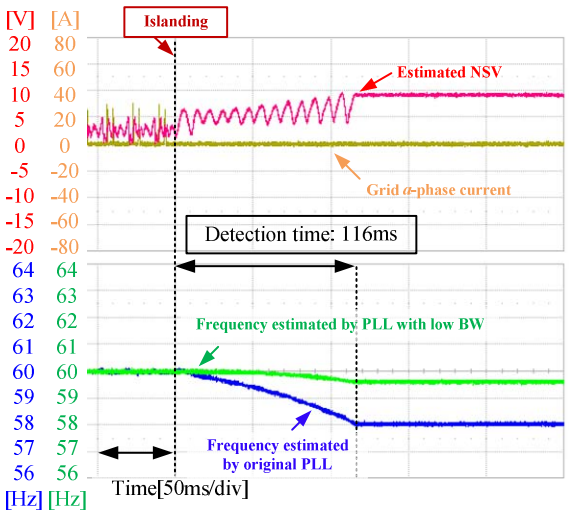
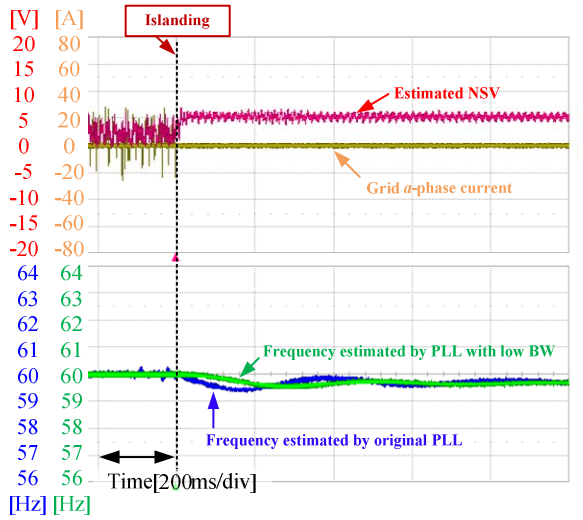
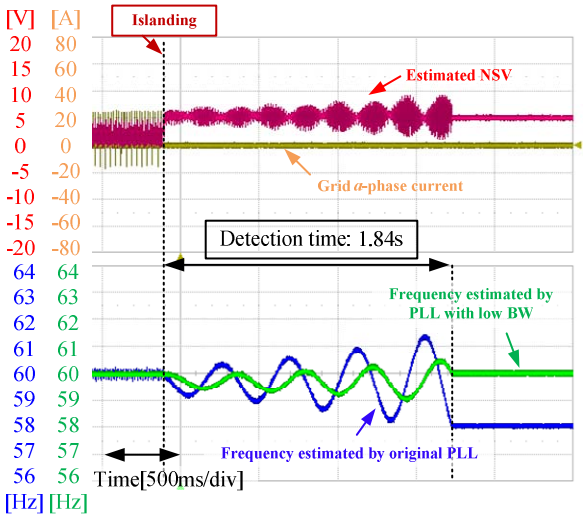


Fig. 13. Experimental result – single inverter with NSV acceleration ($w = 0.15$)



(a) $w = 0.2$



(b) $w = 0.25$

Fig. 14. Experimental results – parallel inverters

was diverged and OUF relay was triggered despite of retarded detection time. Thanks to the proposed acceleration factor, the minimum capacity ratio may be

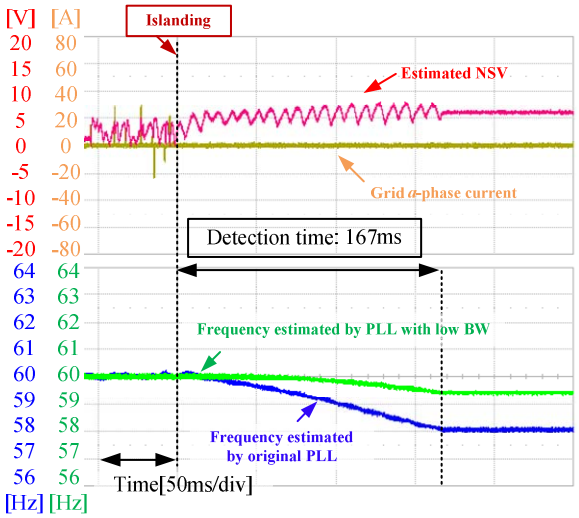


Fig. 15. Experimental result – parallel inverters with NSV acceleration ($w = 0.15$)

reduced under unbalanced load. In Fig. 13, despite of a minute unbalance of load, the acceleration factor shows outstanding detection capability even under capacity ratio 0.15 which is considerably smaller than the minimum capacity ratio of conventional anti-islanding.

To verify discussion for multiple DG system in section III, two inverters as in Fig. 5 (a) are installed and tested. Without NSV acceleration, the inverter with the capacity ratio with 0.2 cannot drift the frequency to trigger OUF relay and that with 0.25 can. As shown in Fig. 14, the divergence of the parallel inverter is similar to the single inverter's results. These experimental results show the validity of the NDZ analysis based on the model replacing multi-inverters to a single virtual inverter. In Fig. 15, the test results of the parallel operation of the inverters with the capacity ratio with 0.15, which is less than the case in Fig. 14 where detection fails, are shown. From the figure, it can be seen that the proposed acceleration can shrink the NDZ in parallel inverters thanks to the utilization of negative sequence voltage, even under lower capacity ratio than minimum value of conventional method.

V. Conclusions

The acceleration factor exploiting negative sequence component of the grid voltage, has conspicuously enhances the performance of islanding-detection with very small unbalanced load condition. The proposed acceleration factor can be adopted in any positive feedback type of anti-islanding. In this paper, especially one of the frequency feedback methods has been implemented and the acceleration reveals improvements of detection time and NDZ under unbalanced islanding-loads.

The guide line of the tuning of the feedback gain for the frequency drift has been derived while keeping the power factor regulation of the grid at normal operation. By replacing the nominal frequency with the frequency estimated by an additional low bandwidth PLL, the reactive power in the steady state at normal grid

connected operation can be minimized.

The approach to analyze NDZ of the proposed algorithm in multiple DG system has been also discussed. By analyzing NDZ of equivalent single virtual inverter, the NDZ of multiple DG system also would be analyzed. The results in simulation and experiment show that the dynamics of parallel-inverters follow that of the single inverter which has same capacity ratio. Especially, in unbalanced load, the proposed algorithm overcomes the minimum capacity ratio of conventional anti-islanding and shrinks the NDZ conspicuously.

APPENDIX

In both simulation and experiment, the capacitance of the capacitor of balanced load was adjusted in order to maintain grid frequency on nominal value after islanding.

TABLE I
PARAMETERS IN SIMULATION

Grid voltage			220 V
Grid frequency			60Hz
Rated power			5 kW
Balanced load (Q_f = 2.5)		R	9.68 Ω
		L	10.3 mH
		C	680 μF
Type 1	Balanced load	R	10.65 Ω
		L	11.3 mH
		C	613.5 μF
	Three phase rectified load		320 Ω
	Single phase rectified load		160 Ω
Type 2	Balanced load	R	9.68 Ω
		L	2.14 mH
		C	3.28 mF
	Three phase rectified load		320 Ω
	Single phase rectified load		160 Ω
Balanced load (Q_f = 8.5)		R	9.68 Ω
		L	3.02 mH
		C	2.32 mF
Balanced load (Q_f = 9.5)		R	9.68 Ω
		L	2.70 mH
		C	2.60 mF

TABLE II
PARAMETERS IN EXPERIMENT

Nominal grid voltage		220 V
Nominal grid frequency		60Hz
Rated power of entire system		5 kW
Islanding load (Q_f = 2, f_{res} = 59.6 Hz)	R	9.68 Ω
	L	12.8 mH
	C	580 μF
Bandwidth of original PLL		20 Hz
Bandwidth of additional PLL		2 Hz

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