Common-mode Voltage Reduction of Three Level Four Leg PWM Converter

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***Abstract*— This paper presents a carrier-based Pulse Width Modulation (PWM) method to reduce the common-mode voltage (CMV) of the three level four leg converter. The idea of the proposed PWM method is very intuitive and easy to be understood. Based on the analysis of the Space Vector PWM (SVPWM) and the Sinusoidal PWM (SPWM) switching patterns, 4th leg pole voltage of the three phase converter, so called 'f pole voltage' has been manipulated to reduce the common-mode voltage. To synthesize f pole voltage for the suppression of the CMV, positive and negative pole voltage references of f leg are calculated. Also an offset voltage to prevent the distortion of a, b, c phase voltages regarding to the neutral point is deduced. Not requiring extra hardware, the proposed PWM strategy can be easily implemented in the software of the DSP based converter control system without degradation of the control performance. The three level four leg converter with the proposed PWM algorithm results in a remarkable reduction in peak-to-peak value of the CMV. The feasibility of the proposed PWM method is verified by both simulation and experimental results. From the simulation and the experimental results, the peak-to-peak value of the CMV in the proposed PWM method is 33% comparing to that in the SVPWM method, and the transition number of the CMV during a switching period in the proposed PWM method is only 25% of that in the SVPWM method.**

I. INTRODUCTION

With concerns relating to the energy and the environmental issues, the interest in the distributed generation system is increasing gradually. To interface the variable voltage/frequency distributed generators with the grid, the power converters are commonly used.

In general, for three phase utility system, the two level three leg topology is widely used because of its simple structure and the easiness in control. However, the multi-level topologies are getting attentions owing to smaller filters and higher efficiency compared to the two level topology. Among the multi-level converters, the three level converters like Neutral Point Clamped (NPC) topology or T-type topology are most popular because of their relatively simple control and technical maturity [1, 2].

In the normal state where the converter is connected to the three phase grid, the three leg converter does not make any problem whether three phase loads are balanced or not. But in the abnormal state when the converter is disconnected to the grid because of the grid faults or any other reason, the phase voltages in the conventional three leg converter are affected by the load condition. In the extreme case where only 2 same single phase loads are connected between two phases, the two phase voltages of the loads would not be $V_{l-l}/\sqrt{3}$ but be $V_{l-l}/2$. Such voltages are not acceptable even during a few periods of the grid voltage. To handle this unbalanced load conditions in the stand-alone operation of the converter, three leg converters could be operated as three single phase half bridge converters, that is, three leg four wire structure, at the cost of the reduced output ac voltage. Likewise, a transformer could be located between the converter and external loads at the cost of efficiency, size and weight. With the development of the power semiconductors, the cost to power ratio of the power semiconductor has dropped continuously. Thus the four leg topologies, which has an extra leg usually being connected to the neutral point of the grid and that of the loads via filter, would be a solution to handle these unbalanced three phase load conditions [3].

Regardless of the number of levels and legs, the common-mode voltage (CMV) always exists in the PWM power converters because of its switching operation. The high frequency CMV causes common-mode current (CMC) via parasitic capacitor components between the converter, loads, cables and the ground, respectively. The CMC would be a source of consequent electromagnetic interference (EMI) noise and it may result in the malfunction of the converter control system and in the interference with other electronic equipment in the vicinity of the converter [4]. Due to the increase of the PWM switching frequency in the application

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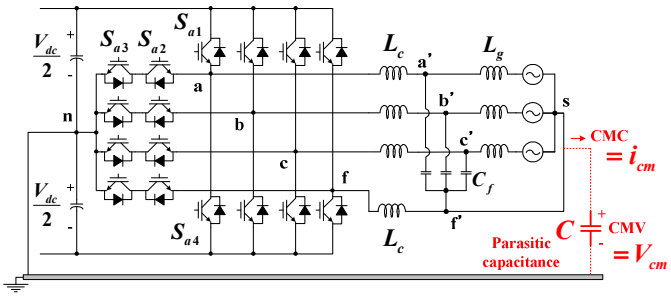

Figure 1. System configuration of 3 level 4 leg converter

field, the occurrence of such problems has been increasing. So the CMV reduction techniques have been getting a lot of attention. The CMV and resulting CMC can be reduced passively and actively. Passive methods include adopting the magnetic circuits such as the common-mode inductor or the common-mode transformer [5-7]. But additional magnetic circuits have cost and size penalties. Active methods are divided into three ways. First, additional active circuits involving transistors [8] can be utilized. Second, the multi-level topology such as NPC [9] may be used. Because it has multi pole voltage levels, the CMV is inherently reduced. Third way is to manipulating the PWM pattern without any additional circuit. It can be implemented only by modifying the software. And, majority of the recent researches for the CMV reduction have focused on the PWM methods which is called Reduced CMV-PWM (RCMV-PWM) methods. Most of the RCMV-PWM methods are about the two level three leg converters [10-15]. Only a few researches are about the three level three leg topology [9] and the two level four leg topology [16, 17].

In this paper, carrier-based PWM methods are presented for the CMV reduction in the three level four leg topology as shown in Fig. 1. Also the corresponding offset voltages are proposed to prevent harmonic voltages in the output voltage of the converter. To evaluate the proposed PWM methods, their performance are analyzed. The simulation and the experimental results verify the performances of the proposed PWM methods.

II. Common-mode Voltage of Three Level Four Leg Converter

The CMV of the four leg converter can be expressed as (1) [16].

$$V_{sn} = \frac{V_{an}+V_{bn}+V_{cn}+V_{fn}}{4}. \quad (1)$$

The CMV in (1) can be rewritten by four leg switching states (S_a, S_b, S_c, S_f) of the three level topology and the CMV state (S_{CMV}).

$$V_{sn} = \frac{S_a+S_b+S_c+S_f}{4}\frac{V_{dc}}{2} = \frac{S_{CMV}}{4}\frac{V_{dc}}{2} \quad (2)$$

, where

$$S_x = \begin{cases} 1, & S_{x1} = on \\ 0, & S_{x2,3} = on, x = a,b,c,f \\ -1, & S_{x4} = on \end{cases} \quad (3)$$

and

$$S_{CMV} = S_a + S_b + S_c + S_f. \quad (4)$$

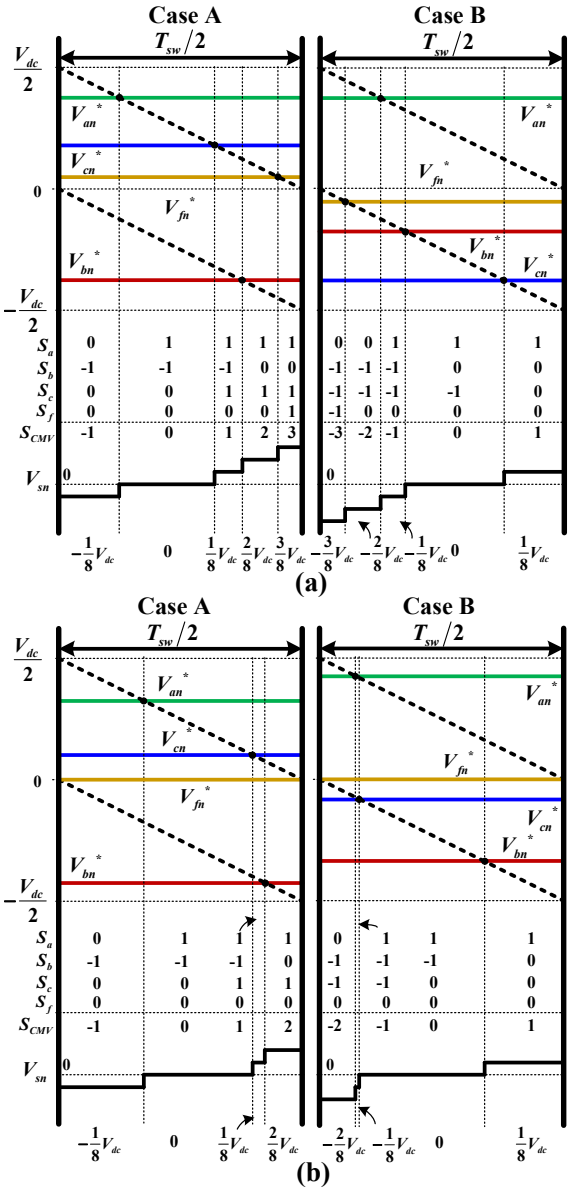

Figure 2. Switching patterns and CMV (a) of SVPWM, (b) of SPWM

If the carrier-based SVPWM method using an offset voltage for four leg system described in [18] is applied, S_{CMV} has seven distinct values, namely, -3, -2, -1, 0, 1, 2, 3. Then the corresponding CMV would be $-\frac{3}{8}V_{dc}$, $-\frac{2}{8}V_{dc}$, $-\frac{1}{8}V_{dc}$, 0, $\frac{1}{8}V_{dc}$, $\frac{2}{8}V_{dc}$, $\frac{3}{8}V_{dc}$ as shown in Fig. 2 (a). If the SPWM method is applied, the CMV would be $-\frac{2}{8}V_{dc}$, $-\frac{1}{8}V_{dc}$, 0, $\frac{1}{8}V_{dc}$, $\frac{2}{8}V_{dc}$ as shown in Fig. 2 (b).

Based on the analysis of the switching patterns in the SPWM method, two fixed rules about S_{CMV} could be found. One rule is that S_{CMV} at the initial part of carrier wave, where both carrier waves are at their peak, would be always -1 or -2 as in Fig. 2 (b). In case of 'Case A', when initial value of S_{CMV} is -1, two of three a, b, c pole voltage references are positive. In case of 'Case B', when that of

S_{CMV} is -2, one of those is positive. The other is that S_{CMV} increases one by one at every crossing point of reference pole voltages and triangular carrier waves.

III. PROPOSED PWM METHOD TO SUPRESS CMV

A. Concept of Proposed PWM Method

To reduce the CMC, it is important to decrease not only the magnitude of the CMV but also the number of the transition of the CMV during a switching period.

Based on the two rules about S_{CMV} as mentioned above, S_f can be manipulated adequately so as S_{CMV} to be as small as possible. Assuming that SPWM method is applied, S_{CMV} in case of 'Case A' and 'Case B' are -1, 0, 1, 2 and -2, -1, 0, 1 respectively. If S_f is 1, 0, -1, -2 and 2, 1, 0, -1 in each case, S_{CMV} is always 0, 0, 0, 0. It means that the CMV is 0V and there is no CMC. But S_f cannot be 2 or -2 practically in the three level topology from the equation (3). So the possible value of S_f to minimize the CMV is 1, 0, -1, -1 and 1, 1, 0, -1. Finally, overall S_{CMV} in each case is 0, 0, 0, 1 and -1, 0, 0, 0 in sequence as shown in Fig. 3. The CMV would be 0, 0, 0, $\frac{1}{8}V_{dc}$ and $-\frac{1}{8}\mathrm{V_{dc}}$, 0, 0, 0. It means the CMV changes only once during a half of the switching period ($T_{sw}/2$) and the peak-to-peak value of the CMV is limited only to $\frac{1}{4}V_{dc}$.

B. Implementation of Proposed PWM Method

To implement S_f as desired, the pole voltage of the extra leg, f leg, should have 3 values ($\frac{1}{2}V_{dc}$, 0, $-\frac{1}{2}V_{dc}$) in sequence at every $T_{sw}/2$ unlike those($-\frac{1}{2}V_{dc}$, 0 or 0, $\frac{1}{2}V_{dc}$) of a, b, c legs as in Fig. 3.

Because two carrier waves exist in the three level topology, it is possible to implement f leg pole voltage by modifying the conventional PWM method in Fig. 4 (a) to proposed method in Fig. 4 (b). At the first, the carrier waves' phases

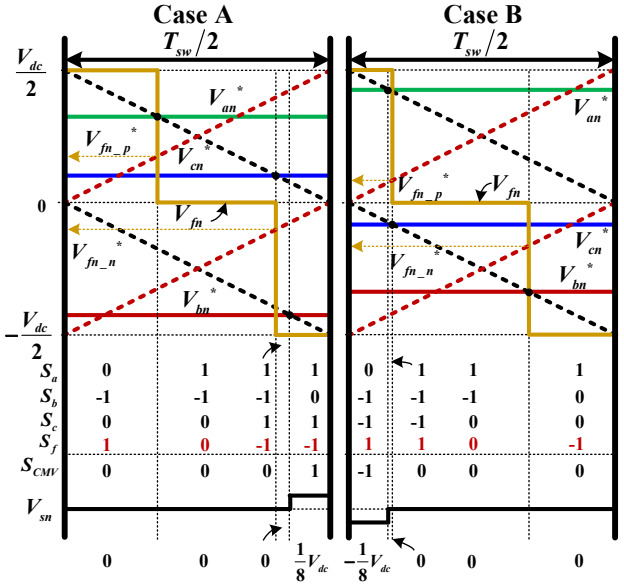

Figure 3. Switching patterns and CMVs of the proposed PWM (PPPWM1)

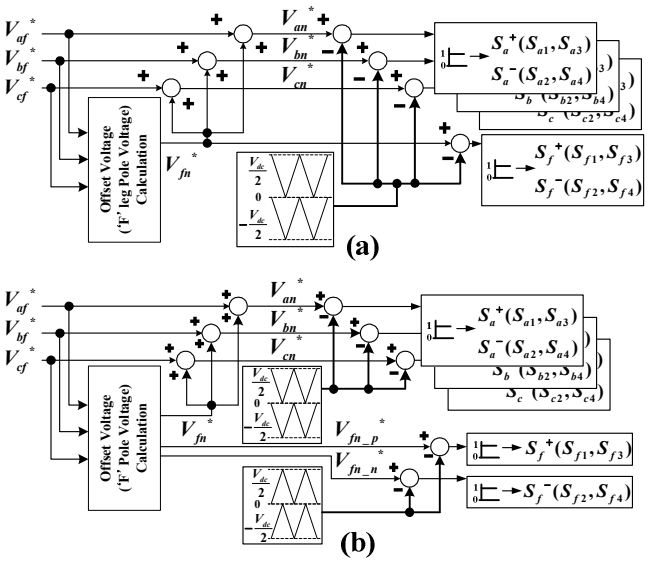

Figure 4. Block diagram of (a) conventional PWM method, (b) proposed PWM methods for CMV suppression

of f leg should be shifted to 180° comparing to those of a, b, c legs to accommodate the reverse state order of f leg pole voltage. The other one to modify is that two f pole voltage references ($V_{fn\_p}{}^*$, $V_{fn\_n}{}^*$) are needed for double switching operation of f leg during $T_{sw}/2$, which are corresponding to upper carrier wave and lower carrier wave, respectively.

In 'Case A' of Fig. 3, $V_{fn\_p}{}^*$ should be equal to $\frac{V_{dc}}{2} - V_{an}{}^*$, and $V_{fn\_n}{}^*$ should be equal to $-V_{cn}{}^*$. $V_{fn\_p}{}^*$, $V_{fn\_n}{}^*$ can be generally expressed as (5) in 'Case A'.

$$\begin{cases} V_{fn\_p}{}^* = \frac{V_{dc}}{2} - V_{\mathrm{max\_pole}}{}^p \\ V_{fn\_n}{}^* = -V_{\mathrm{mid\_pole}}{}^p \end{cases} \tag{5}$$

, where

$$\begin{cases} V_{\mathrm{max\_pole}}{}^p = \max(V_{\mathrm{an}}{}^p, V_{\mathrm{bn}}{}^p, V_{\mathrm{cn}}{}^p) \\ V_{\mathrm{mid\_pole}}{}^p = \mathrm{mid}(V_{\mathrm{an}}{}^p, V_{\mathrm{bn}}{}^p, V_{\mathrm{cn}}{}^p) \\ V_{\mathrm{min\_pole}}{}^p = \min(V_{\mathrm{an}}{}^p, V_{\mathrm{bn}}{}^p, V_{\mathrm{cn}}{}^p) \end{cases} \tag{6}$$

and

$$V_{\mathrm{xn}}{}^p \triangleq \begin{cases} V_{\mathrm{xn}}{}^*, & V_{\mathrm{xn}}{}^* \geq 0 \\ V_{\mathrm{xn}}{}^* + \frac{V_{\mathrm{dc}}}{2}, & V_{\mathrm{xn}}{}^* < 0 \end{cases}, \mathrm{x} = \mathrm{a, b, c}\,. \tag{7}$$

In the same way, $V_{fn\_p}{}^*$, $V_{fn\_n}{}^*$ can also be generally expressed as (8) in 'Case B'.

$$\begin{cases} V_{fn\_p}{}^* = \frac{V_{dc}}{2} - V_{\mathrm{mid\_pole}}{}^p \\ V_{fn\_n}{}^* = -V_{\mathrm{min\_pole}}{}^p \end{cases}. \tag{8}$$

Applying f pole voltage references like (5) and (8), the CMV can be reduced as small as possible.

However, the average pole voltage of f leg, which is connected to neutral point ('s' in Fig. 1) through an inductor, is not null during $T_{sw}/2$. So three a, b, c phase voltages, defined as the voltages between each phase and neutral point, would inevitably include harmonic components owing to the nonzero average f leg pole voltage. As a result of the harmonic voltages, there would be harmonic currents in each phase. Hence, a certain offset voltage ($V_{fn}{}^*$) should be added to the phase reference voltages in Fig. 4 (b) to

nullify the harmonic voltages from the nonzero average f leg pole voltage.

In 'Case A', average f leg pole voltage ($V_{fn\_average}$) can be deduced as (9).

$$V_{fn\_average} = \frac{V_{dc}}{2} - V_{\max\_pole}{}^{p} - V_{\mathrm{mid}\_pole}{}^{p} . \quad (9)$$

In (9), $V_{fn\_average}$ should be equal to $V_{fn}{}^{*}$. If an offset voltage to nullify harmonic voltages is added to each of the phase voltage references, an equation (10) can be obtained.

$$V_{fn}{}^{*} = \frac{V_{dc}}{2} - \left(V_{\max\_phase}{}^{p} + V_{fn}{}^{*}\right) - \left(V_{\mathrm{mid}\_phase}{}^{p} + V_{fn}{}^{*}\right) \quad (10)$$

, where

$$\begin{cases} V_{\max\_\mathrm{phase}}{}^{p} = \max(V_{\mathrm{af}}{}^{p}, V_{\mathrm{bf}}{}^{p}, V_{\mathrm{cf}}{}^{p}) \\ V_{\mathrm{mid}\_\mathrm{phase}}{}^{p} = \mathrm{mid}(V_{\mathrm{af}}{}^{p}, V_{\mathrm{bf}}{}^{p}, V_{\mathrm{cf}}{}^{p}) \\ V_{\min\_\mathrm{phase}}{}^{p} = \min(V_{\mathrm{af}}{}^{p}, V_{\mathrm{bf}}{}^{p}, V_{\mathrm{cf}}{}^{p}) \end{cases} \quad (11)$$

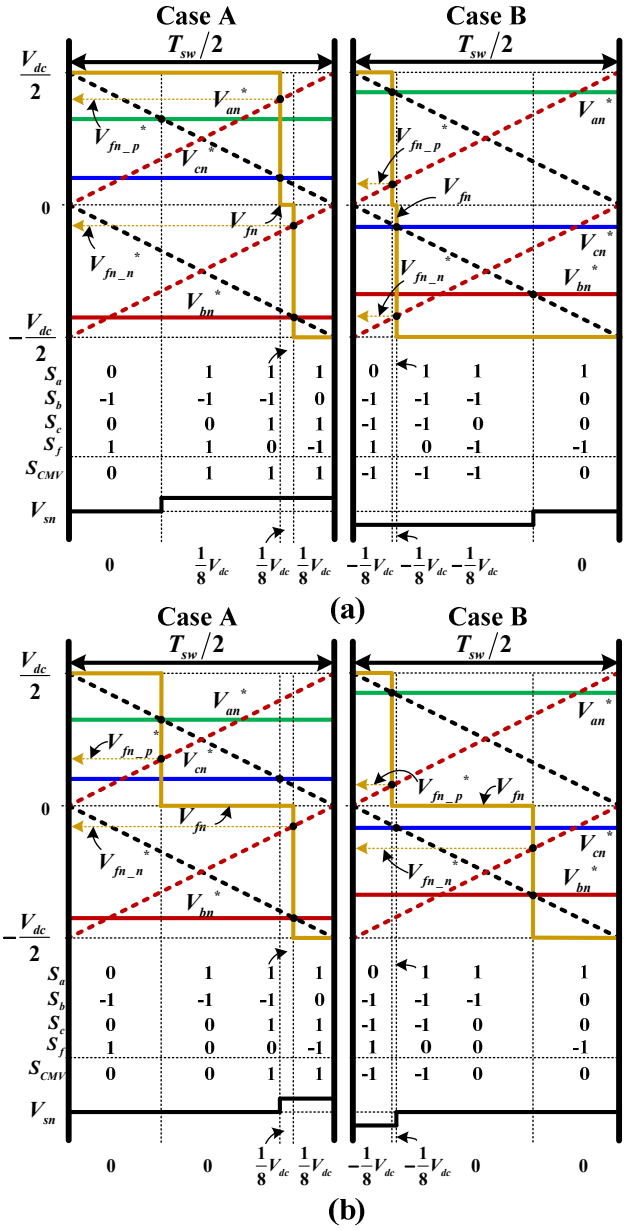

Figure 5. Switching patterns and CMVs of proposed PWMs (a) PPPWM2, (b) PPPWM3

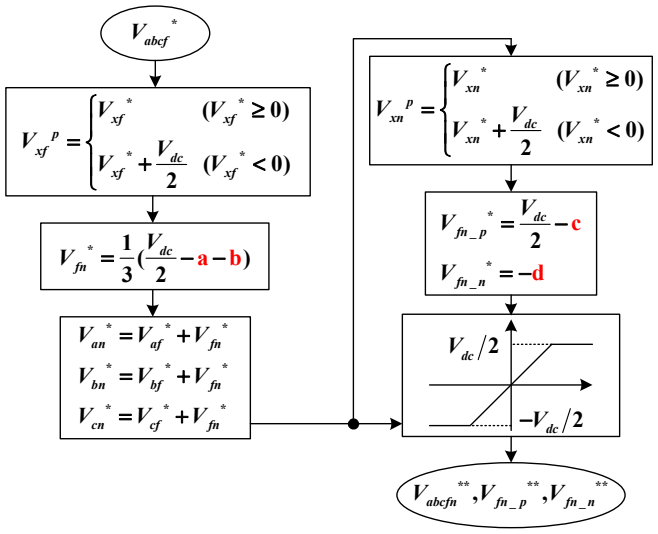

Figure 6. Flowchart of PPPWM methods (a,b,c,d are specified in table I according to each PPPWM method)

and

$$V_{\mathrm{xf}}{}^{p} \triangleq \begin{cases} V_{\mathrm{xf}}{}^{*} & , V_{\mathrm{xf}}{}^{*} \geq 0 \\ V_{\mathrm{xf}}{}^{*} + \frac{V_{\mathrm{dc}}}{2} & , V_{\mathrm{xf}}{}^{*} < 0 \end{cases}, \mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}. \quad (12)$$

From the equation (10), the offset voltage nullifying the harmonic voltages can be derived as (13) in 'Case A'.

$$V_{\mathrm{fn}}{}^{*} = \frac{1}{3}\left(\frac{V_{dc}}{2} - V_{\max\_\mathrm{phase}}{}^{p} - V_{\mathrm{mid}\_\mathrm{phase}}{}^{p}\right) . \quad (13)$$

In the similar way, the offset voltage of 'Case B' can be derived as (14).

$$V_{\mathrm{fn}}{}^{*} = \frac{1}{3}\left(\frac{V_{dc}}{2} - V_{\mathrm{mid}\_\mathrm{phase}}{}^{p} - V_{\min\_\mathrm{phase}}{}^{p}\right) . \quad (14)$$

C. *Other PWM Methods*

The proposed PWM method above-mentioned is called 'Push-Pull PWM1 (PPPWM1)' hereafter.

The switching of f leg in PPPWM1 method happens at the first and second switching points of a, b, c leg in 'Case A'. However, the switching can be changed differently. The variations of f leg switching instants may be named as PPPWM2 and PPPWM3 method. In 'Case A', the switching of f leg occurs at the second and third points in PPPWM2 and at the first and third points in PPPWM3. In 'Case B', similarly, the switching of f leg is different according to PPPWM1, PPPWM2, and PPPWM3, respectively.

The switching patterns and the CMVs in case of the PPPWM2 and PPPWM3 method are shown in Fig. 5. The shapes of the CMVs are different depending on the PPPWM methods. But the number of the CMV transition is one

TABLE I. VALUES FOR FLOWCHART IN FIG. 6

Item	Case	a	b	c	d
PPPWM1	A	$V_{\max\_phase}{}^{p}$	$V_{\mathrm{mid}\_phase}{}^{p}$	$V_{\max\_pole}{}^{p}$	$V_{\mathrm{mid}\_pole}{}^{p}$
	B	$V_{\mathrm{mid}\_phase}{}^{p}$	$V_{\min\_phase}{}^{p}$	$V_{\mathrm{mid}\_pole}{}^{p}$	$V_{\min\_pole}{}^{p}$
PPPWM2	A	$V_{\mathrm{mid}\_phase}{}^{p}$	$V_{\min\_phase}{}^{p}$	$V_{\mathrm{mid}\_pole}{}^{p}$	$V_{\min\_pole}{}^{p}$
	B	$V_{\max\_phase}{}^{p}$	$V_{\mathrm{mid}\_phase}{}^{p}$	$V_{\max\_pole}{}^{p}$	$V_{\mathrm{mid}\_pole}{}^{p}$
PPPWM3	A	$V_{\max\_phase}{}^{p}$	$V_{\min\_phase}{}^{p}$	$V_{\max\_pole}{}^{p}$	$V_{\min\_pole}{}^{p}$
	B				

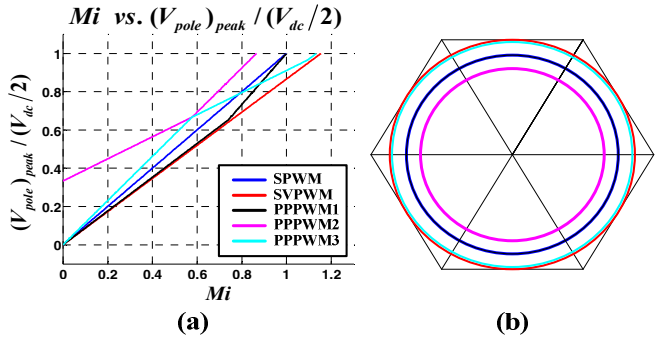

Figure 7. (a) Relationship of Mi and pole voltge normalized by $V_{dc}/2$, (b) Voltage linearity limits

during $T_{sw}/2$ in all PPPWM methods. Considering the relationship of the CMV and the CMC as equation (15), all CMCs happen only once during $T_{sw}/2$.

$$i_{\mathrm{cm}} = C\frac{dV_{cm}}{dt}. \tag{15}$$

Fig. 6 shows PPPWM methods' flowchart and their values, a, b, c, d in the flowchart, depending on the PWM methods are listed in Table I.

IV. Performance of The Proposed PWM Method

The performances of various PWM methods are investigated using the PWM evaluation tools in [12, 19]. Those contain the voltage linearity and the Harmonic Distortion Factor (HDF).

A. Voltage Linearity

In this paper, the voltage utilization level, i.e., the modulation index, is defined as equation (16). It is the ratio of the fundamental component magnitude of the phase voltage to the half of the dc-link voltage, which is different from that of [19].

$$\mathrm{Mi} \triangleq \frac{V_{1m}}{V_{dc}/2} \tag{16}$$

The outer region of the voltage linearity limit is so called as the over-modulation region. In the over-modulation region, the output voltage magnitude is always less than the reference value, so it leads to poor output waveform quality and poor dynamic performance. Therefore, the PWM method with wider linear modulation range is preferred.

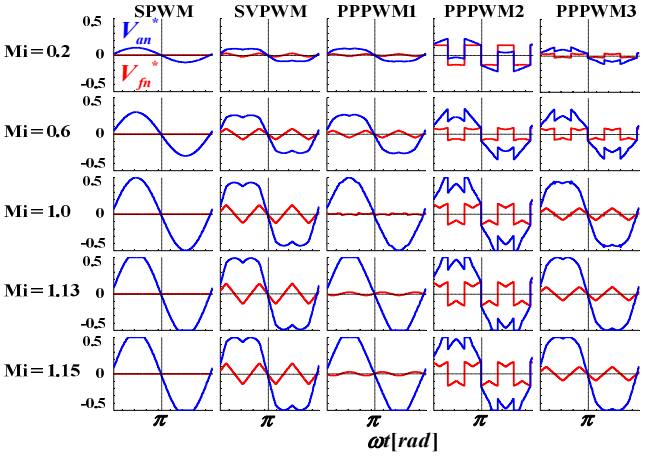

Figure 8. Normalized by V_{dc}, 'a' leg pole voltage and offset voltage

The relationship between Mi and the peak magnitude of the pole voltages is shown in Fig. 7 (a), and the voltage linearity limits of various PWM methods are depicted in Fig. 7 (b). The waveforms of the 'a' leg pole voltages and their offset voltages of various PWM methods according to some Mis are shown in Fig 8.

The PPPWM1 method has the same voltage linearity characteristics ($0 \le \mathrm{Mi} \le 1$) as the SPWM method. However, the PPPWM2 method has poor voltage linearity range ($0 \le \mathrm{Mi} \le \frac{\sqrt{3}}{2} = 0.866$). But the voltage linearity range of the PPPWM3 method is $0 \le \mathrm{Mi} \le \frac{3}{\sqrt{7}} (= 1.1139)$, which is almost the same as that ($0 \le \mathrm{Mi} \le \frac{2}{\sqrt{3}} (= 1.1547)$) of the SVPWM method.

B. Harmonic Distortion Factor (HDF)

The output voltage of the inverter has inevitable harmonic voltage because of its switching behavior. The harmonic voltage, the difference of the reference voltage (V^*) and output voltage (V_k) vector, results in the current ripple. In [12], the harmonic flux of the two level three leg system is investigate based on the assumption of the inductance load model. In the same manner, the harmonic flux of the three level four leg is studied using the same equation as (17) which means that of N[th] cycle of the PWM.

$$\lambda_h(M_i, \theta, V_{dc}) = \int_{NT_{sw}}^{(N+1)T_{sw}} (V_k - V^*)dt. \tag{17}$$

But the voltage vector of three level four leg topology contains zero sequence component (V_n) as equation (18) unlike that of the two level three leg topology.

$$V = \begin{bmatrix} V_d \\ V_q \\ V_n \end{bmatrix} = \begin{bmatrix} \frac{2}{3}V_a - \frac{1}{3}V_b - \frac{1}{3}V_c \\ \frac{\sqrt{3}}{3}V_b - \frac{\sqrt{3}}{3}V_c \\ \frac{1}{3}V_a + \frac{1}{3}V_b + \frac{1}{3}V_c \end{bmatrix}. \tag{18}$$

λ_{hn}, normalizing λ_h by a certain flux, can be expressed as (19).

$$\lambda_{hn} = \frac{\pi}{V_{dc}T_{sw}}\lambda_h. \tag{19}$$

The harmonic flux trajectories of various PWM methods when Mi and the reference voltage angle are 0.6 and 30° are depicted in Fig. 9. The smaller the length from the origin

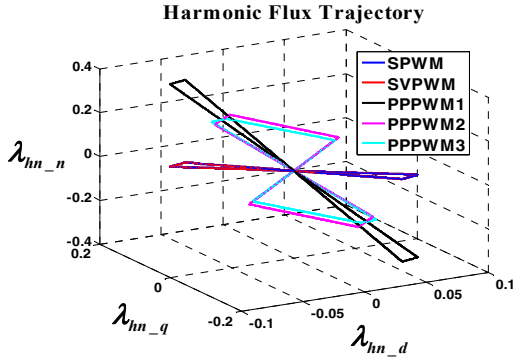

Figure 9. Harmonic flux trajectory of various PWM methods in 3 level 4 leg converter

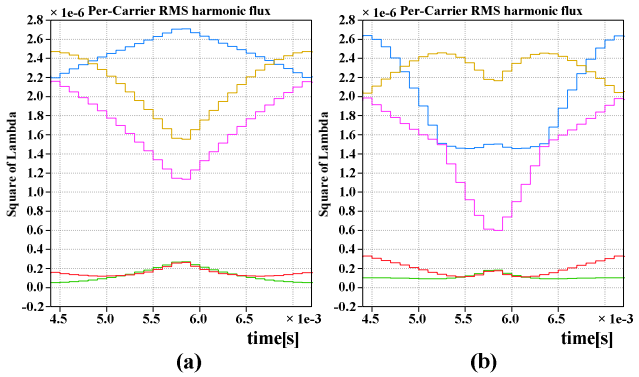

Figure 10. Square of Lambda (a) for Mi = 0.50, (b) for Mi = 0.86 (Green: SPWM, Red: SVPWM, Blue: PPPWM1, Yellow: PPPWM2, Pink: PPPWM3)

(0,0,0) is, the smaller the flux ripple is.

The normalized harmonic flux vector RMS value over a PWM cycle is calculated as follows.

$$\lambda_{hn\_rms}(M_i,\theta) = \sqrt{\int_{T_{sw}} |\lambda_{hn}|^2 dt} \qquad (20)$$

The per-carrier RMS harmonic fluxes are calculated using MATLAB simulation tool for Mi = 0.50 and Mi = 0.86 which are shown in Fig. 10. The PPPWM methods provide higher harmonic flux square-RMS value than the conventional PWM and the PPPWM3 provides the lowest one among 3 PPPWM methods.

Averaging the RMS harmonic flux over the full fundamental cycle and scaling it with $288/\pi^2$, the HDF can be calculated as equation (21) [12].

$$HDF = f(M_i) = \frac{288}{\pi^2}\frac{1}{2\pi}\int_0^{2\pi} {\lambda_{hn\_rms}}^2 d\theta \qquad (21)$$

As shown in Fig. 11, the PPPWM3 method provides the lowest HDF among the PPPWM methods.

The performances of the PPPWM methods are compared to those of conventional SPWM, SVPWM in Table II. In general, the PPPWM3 method shows the best performances among the 3 PPPWM methods. Furthermore, considering that the 4 leg converter is usually used for the interface of the grid, the operation in high Mi, that is, wider linear modulation range, is the most valuable asset. In this sense, the PPPWM3 method would be the best PWM method for the 3 level 4 leg converters to minimize the CMV and the CMC.

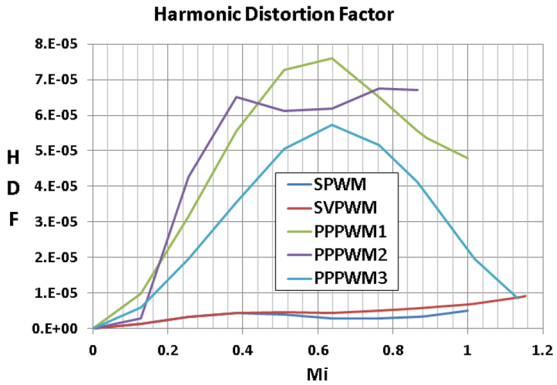

Figure 11. Harmonic Distortion Factor (HDF) according to each PWM method

TABLE II. PERFORMANCE COMPARISON OF VARIOUS PWM METHODS IN 3LEVEL 4 LEG CONVERTER

	SVPWM	SPWM	PPPWM 1	PPPWM 2	PPPWM 3
HDF (Middle Mi)	Low	Low	High	Moderate	Moderate
HDF (High Mi)	Low	Low	Moderate	High	Low
Voltage linearity limits	1.1547	1	1	0.866	1.1139
CMV_{pk-pk}	$\frac{3}{4}V_{dc}$	$\frac{2}{4}V_{dc}$	$\frac{1}{4}V_{dc}$		
ΔCMV	$\frac{1}{8}V_{dc}$				
CMV Switching # per $T_{sw}/2$	4	3	1		

V. SIMULATION RESULTS

The simulation is executed using the 5 kW 3 level (T-type) 4 leg converter whose circuit is shown in Fig. 1. Its switching frequency is 7 kHz and the dead time is set as 2 μs. The dc-link voltage is 400V and the magnitudes of the grid voltages are set as 220 $V_{l-l,rms}$. The parameters of the LCL filter (L_c , L_g , C_f) are 1.2mH, 0.7mH and 9uF, respectively.

The pole voltages and the CMV based on the PPPWM3 method are shown in Fig. 12 (a), corresponding to 'Case B'. The f leg pole voltage, yellow trace of the upper figure in Fig. 12 (a), varies according to the switching state, S_f, shown in 'Case B' of Fig. 3. The peak-to-peak value of the CMV is $\frac{1}{4}V_{dc}$. But some short pulses in the dotted red circles are seen in the CMV waveform. It is undesirable but inevitable because of simultaneous switching characteristic of f leg.

The CMVs according to various PWM methods are shown in Fig. 12 (b). In Fig. 12 (b), the number of the CMV transition is 4, 3, 1 in the case of SVPWM, SPWM, and PPPWM1, respectively. The magnitudes of the CMV in peak-to-peak value are $\frac{3}{4}V_{dc}$, $\frac{2}{4}V_{dc}$, $\frac{1}{4}V_{dc}$, respectively. However, the magnitude of the CMV variation at each

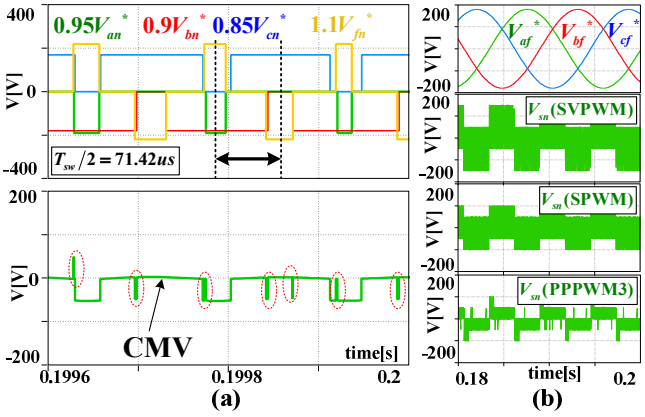

Figure 12. Simulation results (a) Pole voltage references and CMV of PPPWM3, (b) Phase voltage references and CMVs of SVPWM, SPWM and PPPWM3

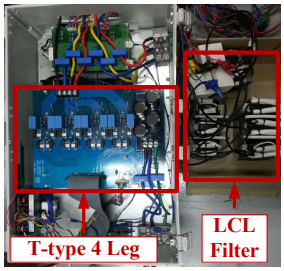

Figure 13. Experimental setup (5kW T-type 4 Leg)

transition is always $\frac{1}{8}V_{dc}$ regardless of the PWM methods.

VI. Experimental Results

A three level four leg converter has been implemented as shown in Fig. 13. A DSP (TMS320C28346) is utilized for the overall control of the converter. The switching frequency and the dead time are the same as those of the simulation. The parameters of experimental set-up in Fig. 13 are the same as those of the simulation.

From Fig. 14 (a), the phase currents are highly distorted when PPPWM3 method is applied without the compensation of $V_{fn}{}^{*}$. The non-zero average voltage of V_{fn} causes the distortion. With the compensation of the harmonic voltage at each pole voltage using the offset voltage given by (13) and (14), the distortion of the phase currents has been disappeared as shown in Fig. 14 (b).

The CMVs of various PWM methods are depicted in Fig. 15 when the converter is supplying the rated power to the grid. The peak-to-peak value of the CMV is $\frac{3}{4}V_{dc}$ (=300V), $\frac{2}{4}V_{dc}$ (=200V) and $\frac{1}{4}V_{dc}$ (=100V) in the case of SVPWM, SPWM and PPPWM1, respectively. Those in case of PPPWM2, PPPWM3 are a little larger than $\frac{1}{4}V_{dc}$ (=100V). Their theoretical values are $\frac{1}{4}V_{dc}$ (=100V) like PPPWM1. The difference comes from the characteristic of the PPPWM methods, simultaneous switching. It is hard to implement simultaneous switching perfectly because of the dead time.

The frequency spectrums of the CMVs in Fig. 15 are

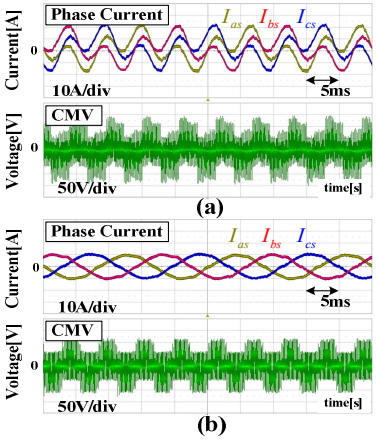

Figure 14. Phase currents and CMV of PPPWM3 (a) when $V_{fn}{}^{*} = 0$., (b) when $V_{fn}{}^{*}$ is properly compensated.

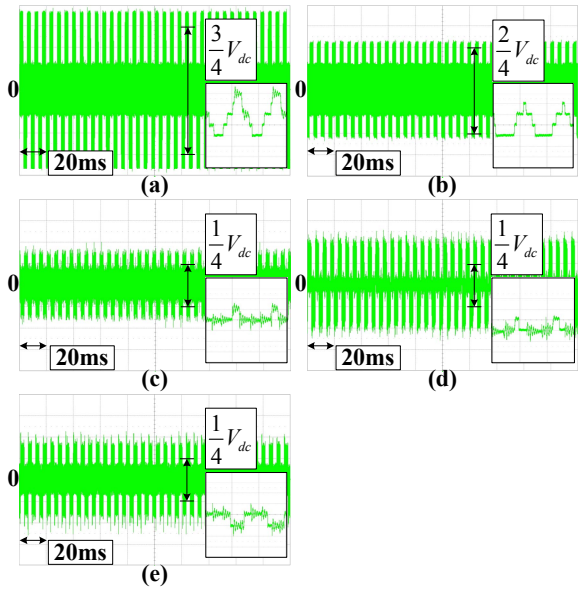

Figure 15. CMV ([50V/div]) at the grid-connected operation mode (a) SVPWM, (b) SPWM, (c) PPPWM1, (d) PPPWM2, (e) PPPWM3

shown in Fig. 16. In each figure, magnified waveform with low frequency range (0 ~ 10 kHz) is inserted. Even if the PPPWM methods are based on the simultaneous switching, the magnitude of the CMV in case of the PPPWM methods is smaller than those in case of the SVPWM and SPWM methods at every harmonic frequency. Among three

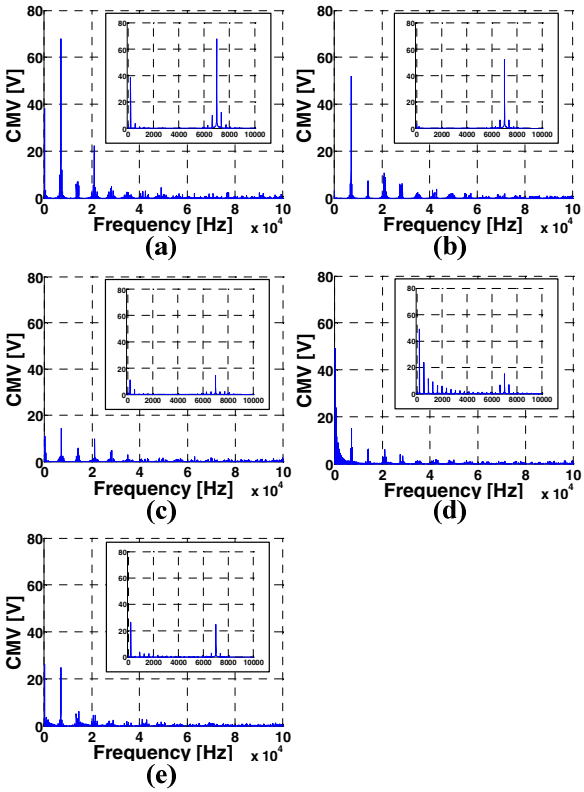

Figure 16. Frequency Spectrum of the CMV in Fig. 15 (a) SVPWM, (b) SPWM, (c) PPPWM1, (d) PPPWM2, (e) PPPWM3

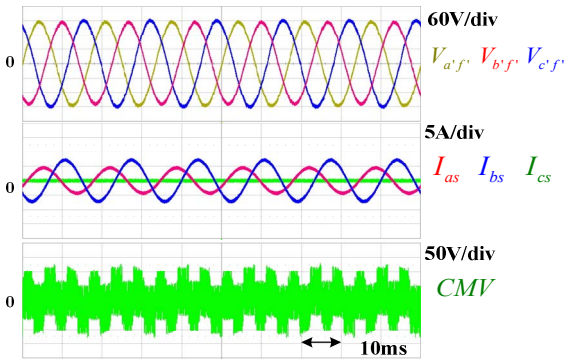

Figure 17. Capacitor voltages, Phase currents and CMV in stand-alone operation when PPPWM3 method is applied.

PPPWM methods, the PPPWM1 method is the best at or below the switching frequency. But the PPPWM3 method is the best over the two times of the switching frequency.

Also the converter is operated in the stand-alone mode which means that the converter solely supply the power to three single phase loads without the grid support. Three single phase loads are unbalanced ($Z_a = 40 + \mathrm{j}2\pi 60 \times 0.05[\Omega]$, $Z_b = 20 + \mathrm{j}2\pi 60 \times 0.025[\Omega]$, $Z_c = \infty[\Omega]$). When the PPPWM3 method is applied, its phase voltages, currents and CMV are shown in Fig. 17. Regardless of the unbalanced loads, the phase voltages are balanced and the CMV is still reduced. The frequency spectrums of the CMVs are also similar to those in Fig. 16.

VII. Conclusion

A carrier-based PWM method to reduce the common-mode voltage of three level four leg converter has been proposed. It is named as Push-Pull PWM (PPPWM) method. There are 3 kinds of the PPPWM methods. The PPPWM methods manipulate extra leg voltage to make the CMV as small as possible. An offset voltage and the voltage references of the additional leg for the PPPWM methods are derived. The performances of the PPPWM and conventional PWM methods are studied. The PPPWM3 method's performance is generally superior to other PPPWM methods. To verify the validity of the PPPWM methods, the simulation and the experiment were carried out. From both simulation and experimental results, it has been confirmed that the peak-to-peak value and the number of transition of the CMVs in case of the PPPWM methods have been reduced by 66% and 75%, respectively comparing to that of the SVPWM method while still keeping harmonic current suppression and almost equivalent linear modulation range to the case of the SVPWM method.

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