A Switching Frequency Reduction and a Mitigation of Voltage Fluctuation of Modular Multilevel Converter for HVDC

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***Abstract*— A switching loss of Modular Multilevel Converter(MMC) might increase drastically in HVDC system because the number of sub-module(SM) is proportional to the DC-link voltage. And, a special strategy for reducing switching frequency has been significant research issue in terms of overall operating efficiency of MMC for HVDC system. The voltage fluctuation of capacitor in SM, however, increases as the switching frequency decreases, and the capacitor with large capacitance which is the main portion of equipment cost for SM is required to mitigate the voltage fluctuation. In this paper, the switching frequency reduction strategy is proposed using the sorting method with a virtual capacitor voltage of individual SMs. In addition, this paper presents the 2nd order harmonic circulating current injection to suppress the voltage fluctuation. By numerical loss analysis, it is identified that the 2nd order harmonic current injection does not incur severe additional loss. Thanks to the harmonic current injection, the capacitance of SM capacitor could be reduced by 33% at the cost of only 0.05 % efficiency degradation in the given simulation condition. To evaluate the effectiveness of the proposed strategies, the computer simulation with 400 kV, 400MA, 221-level MMC has been performed and the results are discussed. Additionally, validity of the proposed strategies has been verified by 7-level down scaled prototype experimental setup.**

Keywords – HVDC, Modular Multilevel Converter, MMC, Switching frequency reduction.

I. INTRODUCTION

Large scale renewable energy power plants have been constructed steadily because of an increased demand for environmental friendly electric power generation. These plants have been enlarged and concentrated in a region where the renewable energy source is abundant such as desserts, valleys and offshores, etc. Moreover, interconnecting power grids between countries is becoming an issue in order to develop mutual benefits with massive integration of renewable energy sources such as "European supergrid" [1],[2]. Voltage Source Converter (VSC) based High Voltage Direct Current (HVDC) transmission system is a feasible and promising solution having ability to transfer the great amount of renewable energy across vast distances with relatively low cost. In addition, HVDC has capability of grid connection without frequency and phase synchronization between different AC grids interconnection of different countries. Modular Multilevel Converter (MMC) is a competitive candidate and attracting worldwide attention for VSC-HVDC [3]. The main advantages of MMC include low harmonic distortion resulting minimum filter requirement, low dv/dt, lower switching frequency, and etc. Especially, MMC presents significant advantages over conventional two -level VSC-HVDC such as modularity with standardized power modules, a simple scaling for an extension to the higher voltage and number of voltage level, and a possibility for eliminating filters [4]-[6].

The main feature of MMC is a cascade connection of the sub-modules (SM) which has relatively low voltage rating. On this characteristic of MMC, a switching loss in HVDC is a significant concern in terms of total loss because the number of SM is proportional to the DC-link voltage. Hence, the switching frequency reduction strategy should be engaged to control principle of MMC for efficient operation of HVDC. In this paper, a novel sorting algorithm reducing the switching frequency of SM is proposed, where balancing of the capacitor voltages of SMs are sorted by the virtual capacitor voltage. The voltage fluctuation of capacitor in SM, however, increases as the switching frequency decreases because the arm current flows through the capacitor of SM for a longer period under the low switching frequency. In this paper, the 2nd order harmonic circulating current injection is also proposed to suppress voltage fluctuation which has been presented in some literatures [7], [17]. It may be concerned that the conduction loss increases due to the additional circulating current. But, in this paper, it is identified by the loss analysis that the 2nd order harmonic current injection does not incur severe additional loss thanks to the non-linearity of saturation voltage of IGBT and diode.

II. MATHEMATICAL MODELING OF MMC

As shown in Fig. 1, per phase equivalent circuit of MMC can be described with the voltage sources of arms, arm currents, phase current and DC bus voltage source. In Fig. 1, i_{xs}, i_{xu}, i_{xl} and i_{xo} stand for the output phase current, the upper arm current, the

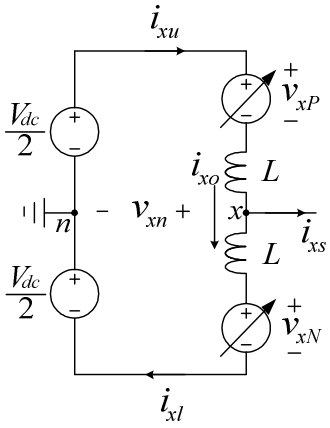


Figure 1. Per phase equivalent circuit of MMC.

lower arm current and the circulating current, respectively, where the notation '*x*' represents phase(*x*=*u*, *v*, or *w*). v_{xP} and v_{xN} stand for the output voltage of upper arm and lower arm, respectively. And v_{xN} stands for the pole voltage where the notation '*n*' represents for the neutral point of DC bus.

The circulating current is defined as the average value of the upper and lower arm currents and the arm current can be deduced with the circulating current and phase current as (1).

$$i_{xo} = 0.5 \cdot (i_{xu} + i_{xl}),\ i_{xu} = 0.5 \cdot i_{xs} + i_{xo},\ i_{xl} = -0.5 \cdot i_{xs} + i_{xo}. \quad (1)$$

According to Kirchhoff's voltage law, the voltage reference of upper and lower arm can be derived as (2) to regulate the circulating current. v_{xo}^* is designated as the leg common voltage in this paper. Also, the arm voltage reference can be determined as (3) to make proper pole voltage reference.

$$v_{xP}^*\big|_{common} = v_{xN}^*\big|_{common} = \frac{V_{dc}}{2} - v_{xo}^*. \quad (2)$$

$$v_{xP}^*\big|_{pole} = -v_{xn}^*,\ v_{xN}^*\big|_{pole} = v_{xn}^*. \quad (3)$$

Overall arm voltage reference can be expressed as (4) from the superposition of (2) and (3) [8].

$$\begin{aligned} v_{xP}^* &= v_{xP}^*\big|_{pole} + v_{xP}^*\big|_{common} = \frac{V_{dc}}{2} - v_{xn}^* - v_{xo}^* \\ v_{xN}^* &= v_{xN}^*\big|_{pole} + v_{xN}^*\big|_{common} = \frac{V_{dc}}{2} + v_{xn}^* - v_{xo}^* \end{aligned}. \quad (4)$$

III. Switching Frequency Reduction Strategy

A. Capacitor voltage balancing algorithm employing sorting method

The circuit configuration of sub-module can be designed by various circuit topologies. As shown in Fig. 2, this paper adopts a half-bridge circuit based SM which is generally used in industrial field [9],[10]. The capacitor current flows through the capacitor in case of '*S*=1' which means that the upper switch of half-bridge is conducting. Thus, the capacitor voltage increases when the upper switch is conducting and the positive current flows to the arm. While, the capacitor voltage decreases while the upper switch is conducting and the negative current flows to the arm. It means that the only conduction state of upper

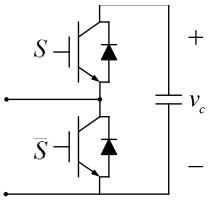


Figure 2. Half-bridge circuit based sub-module.

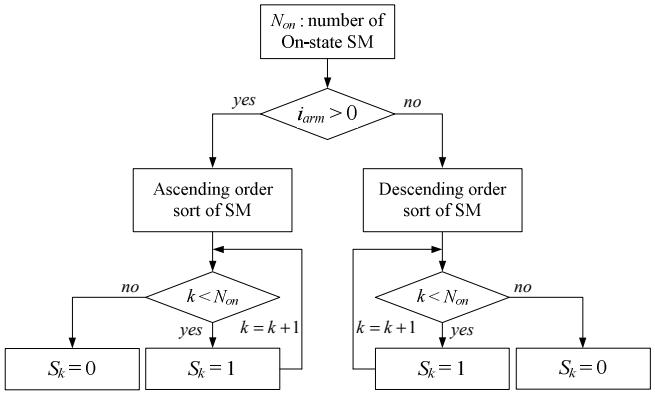


Figure 3. Flow chart of the balancing algorithm.

switch of each SM can affect the capacitor voltage of SM.

In this paper, the conduction state of upper switch of each SM(On-state SM) is defined as the value of the switching function and it is set as '1' and the non-conducting state of upper switch of each SM(Off-state SM) is defined as '0', which means conduction of lower switching devices of the half bridge module. The balancing algorithm employing sorting method has been widely used for the balanced capacitor voltage of SM [11]-[13]. A specific SM which has higher or lower voltage compared to other SM have higher priority to discharge or charge the capacitor, and the balancing of SM for each arm can be achieved. The balancing algorithm can be implemented as follows. First, the duty ratio of arm is calculated from the arm voltage reference. Next, SM is sorted by its capacitor voltage in an ascending or a descending order according to the direction of arm current. Finally, the duty ratio is applied to SM in order sorted.

The switching transition during one sampling period can be avoided by NLC(Nearest Level Control modulation) which has been investigated for multilevel topologies[14]. Fig. 3 shows the simplified flow chart of the balancing algorithm employing sorting method with NLC. In Fig. 3, S_k stands for the switching function of *k*-th sub-module in the arm, and the initial value of *k* is zero. However, the average switching frequency might be increased if the sorting in the balancing algorithm is performed at every sampling point. Therefore, in the worst case, On-state(conducing) SMs and Off-state(non-conducting) SMs can be changed each other in a sampling period, because the capacitor voltage of On-state SM increases or decreases by the arm current while the capacitor voltage of Off-state SM does not change.

B. Switching frequency reduction strategy with virtual capacitor voltage of SM

The changing of On/Off-state SM can be described conceptually as Fig. 4. In Fig. 4, v_x stand for the capacitor

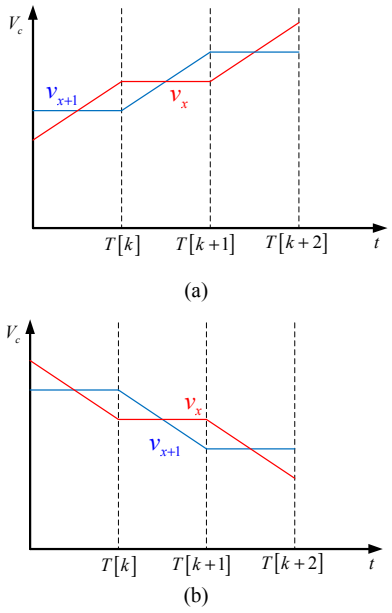


Figure 4. Conceptual graph for sorting process of On/Off-state SM (m=1). (a) positive arm current. (b) negative arm current.

voltage of initial On-state SM while v_{x+1} represent the capacitor voltage of initial Off-state SM. As shown in Fig. 4, the state of SMs is changed when the capacitor voltage of On-state SM is higher or lower than Off-state SM at sampling point. Thus, in the conventional balancing algorithm, the number of switching transition increases by the sorting process.

The transition condition of On/Off-state can be expressed as simple equation as follows. Under the assumption that the arm current is constant during 'm' sampling periods and that the switching state maintains for 'm' sampling periods, the capacitor voltage of On-state SM would vary as (5).

$$v_x[k+m] = v_x[k] + \frac{1}{C}\int_{T[k]}^{T[k+m]} i_{arm}\,dt \approx v_x[k] + m\frac{i_{arm}}{C}T_s, \qquad (5)$$

where T_s stands for sampling period, C stands for capacitance of SM, i_{arm} stands for the arm current, and $T[k] = kT_s$. The capacitor voltage of On/Off-state SM after m sampling period can be expressed as (6), and the switching transition occurs due to the sorting process.

$$\begin{cases} v_x[k+m] > v_{x+1}[k] & (i_{arm} \ge 0) \\ v_x[k+m] < v_{x+1}[k] & (i_{arm} < 0) \end{cases}. \qquad (6)$$

m can be deduced as (7) after substituting (5) to (6).

$$m > \frac{C\left(v_{x+1}[k] - v_x[k]\right)}{i_{arm}T_s}. \qquad (7)$$

Thus, the state of SMs is changed after m-sampling period because the capacitor voltage of On-state SM is higher or lower than Off-state SM. It means that the On/Off-state is kept and the switching transition does not occur during m-sampling period, and it can be noted that the switching frequency decreases as m increases. From (7), m is proportional to the capacitance and inversely proportional to the arm current.

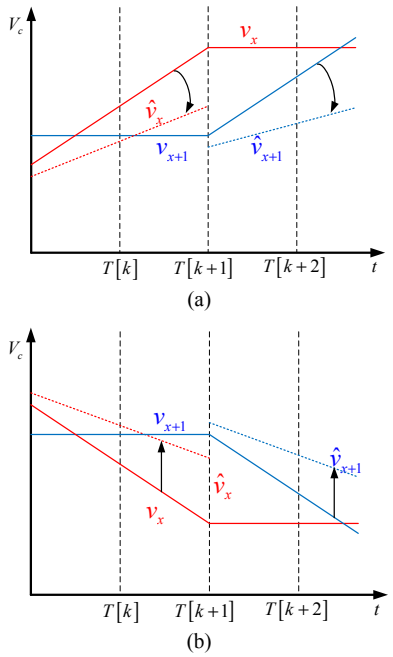


Figure 5. Conceptual graph for sorting process of On/Off-state SM with virtual capacitor voltage (m = 1 ➔ m = 2). (a) positive arm current. (b) negative arm current.

In this paper, the switching reduction strategy is proposed using these characteristics. The state of SM is changed if the capacitor voltage of On-state SM is higher or lower than Off-state SM at each sampling point. Therefore, it is possible to control m if the virtual capacitor voltage, not the real capacitor voltage, of On-state SM is compared with the capacitor voltage of Off-state SM. The virtual capacitance or virtual initial voltage can be used to implement the virtual capacitor voltage.

The sorting process with the virtual capacitor voltage can be described conceptually as Fig. 5. In Fig. 5, subscript '^' stand for the virtual capacitor voltage of corresponding SM. As shown in Fig. 5, m would increases if virtual capacitor voltage of On-state SM is intentionally set as a lower or higher value than real capacitor voltage according to the direction of arm current. The virtual capacitor voltage can be expressed as (8).

$$\begin{aligned} \hat{v}_x[k+m_v] &= v_x[k] + \frac{\alpha}{C}\int_{T[k]}^{T[k+m_v]} i_{arm}\,dt + v_{offset} \\ &\approx v_x[k] + \alpha m_v \frac{i_{arm}}{C}T_s + v_{offset} \\ &\approx v_x[k+m_v] + (\alpha - 1)m_v\frac{i_{arm}}{C}T_s + v_{offset} \end{aligned}. \qquad (8)$$

Under the assumption that the switching transition occurs after m_v sampling period, the virtual capacitor voltage of On-state SM and the real capacitor voltage of Off-state SM after m_v sampling period have inequality as (9), and the switching transition occurs due to the sorting process. Thus, m_v can be deduced as (10) with the same manner.

$$\begin{cases} \hat{v}_x[k+m_v] > v_{x+1}[k] & (i_{arm} \ge 0) \\ \hat{v}_x[k+m_v] < v_{x+1}[k] & (i_{arm} < 0) \end{cases}. \qquad (9)$$

$$m_v > \frac{C\left(v_{x+1}[k]-v_x[k]-v_{offset}\right)}{\alpha i_{arm} T_s}. \quad (10)$$

To reduce the switching frequency, $m_v > m$ should be satisfied which means that the switching states (On/Off) are kept for longer sampling periods than that of original sorting process. Thus, the inequalities can be deduced as (11). In other words, it is possible to decrease the average switching frequency with α and v_{offset} satisfying inequality in (11), where α represents the weighting factor for virtual capacitance, and v_{offset} stands for the offset voltage, and the initial voltage of capacitor can be changed with the offset voltage.

$$\begin{cases} v_{offset} < (1-\alpha)\left(v_{x+1}[k]-v_x[k]\right) & (i_{arm} \ge 0) \\ v_{offset} > (1-\alpha)\left(v_{x+1}[k]-v_x[k]\right) & (i_{arm} < 0) \end{cases}. \quad (11)$$

The virtual capacitor voltage for sorting process can be calculated as (12) under the condition of (11).

$$\hat{v}_{cap}^k = v_{cap}^k + S_k\left(\frac{\alpha-1}{C} i_{arm} T_s + v_{offset}\right), \quad (12)$$

where v_{cap}^k stands for the real capacitor voltage of k-th SM, $\hat{v}_{cap}^k$ stands for the virtual capacitor voltage used in sorting process, S_k represents the switching function of k-th SM.

In this paper, in order to minimize information and calculation burden, the weighting factor, α , is fixed '1'. It means that the only offset voltage, v_{offset}, is used for the proposed strategy. In summary, the virtual capacitor voltage of SMs for sorting method can be expressed (13) in order to implement the proposed strategy simply. The virtual voltage of On-state SM and the real voltage of Off-state SM are used for sorting process to reduce the switching frequency.

$$\begin{cases} \hat{v}_{cap}^k = v_{cap}^k - S_k \cdot v_{offset} & (i_{arm} \ge 0) \\ \hat{v}_{cap}^k = v_{cap}^k + S_k \cdot v_{offset} & (i_{arm} < 0) \end{cases}, \quad (13)$$

where $v_{offset} > 0$. Fig. 6 shows the simplified flow chart of the proposed balancing algorithm employing sorting method with the virtual capacitor voltage.

The real voltage fluctuation of capacitor in SM, however, increases as the switching frequency decreases because the arm current flows through the capacitor of SM for a longer period

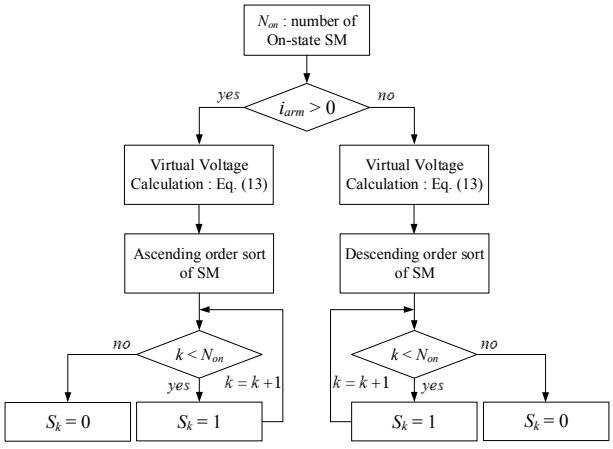


Figure 6. Flow chart of the proposed balancing algorithm.

under the low switching frequency. In this paper, the 2nd order harmonic circulating current injection is also proposed to suppress the voltage fluctuation due to reduced switching frequency.

IV. 2ND HARMONIC CIRCULATING CURRENT INJECTION METHOD

The upper arm and the lower arm power can be calculated as (14) and (15), respectively.

$$P_{xu} = v_{xP}^* i_{xu} \approx \frac{V_{dc}}{2} i_{xo} - v_{xn}^{**} i_{xo} + \frac{V_{dc}}{4} i_{xs} - \frac{1}{2} v_{xn}^{**} i_{xs}. \quad (14)$$

$$P_{xl} = v_{xN}^* i_{xl} \approx \frac{V_{dc}}{2} i_{xo} + v_{xn}^{**} i_{xo} - \frac{V_{dc}}{4} i_{xs} - \frac{1}{2} v_{xn}^{**} i_{xs}. \quad (15)$$

The leg power which is the sum of arm powers can be expressed as (16) neglecting leg common voltage.

$$P_{leg} = P_{xu} + P_{xl} \approx V_{dc} i_{xo} - v_{xn}^* i_{xs}. \quad (16)$$

The leg power can be 'null' when the single phase power is compensated by the circulating current in (17). It means that the common power of upper and lower arm can be eliminated with proper circulating current.

$$i_{xo} = v_{xn}^* i_{xs} / V_{dc} = \frac{V_m I_m}{2V_{dc}} \cos\phi + \frac{V_m I_m}{2V_{dc}} \cos\left(2\omega_s t - \phi\right), \quad (17)$$

where $v_{xn}^* = V_m \cos(\omega_s t)$, and $i_{xs} = I_m \cos(\omega_s t - \phi)$.

The circulating current can be rewritten with a weighting factor, k, of 2nd order harmonic current and Modulation Index($MI = 2V_m/V_{dc}$) as (18).

$$i_{xo} = \frac{I_m}{4} MI \cos\phi + k\frac{I_m}{4} MI \cos\left(2\omega_s t - \phi\right). \quad (18)$$

With the circulating current in (18), the upper arm energy can be calculated as (19).

$$E_{xP} = \frac{V_{dc} I_m}{4\omega_s} \begin{pmatrix} \sin(\omega_s t - \phi) - \frac{MI^2}{2} \cos\phi \sin\omega_s t \\ + \frac{MI}{4}(k-1)\sin\left(2\omega_s t - \phi\right) \\ -k\frac{MI^2}{4}\sin(\omega_s t - \phi) - k\frac{MI^2}{12}\sin\left(3\omega_s t - \phi\right) \end{pmatrix}. \quad (19)$$

Fig. 7 shows the maximum upper arm energy normalized by $V_{dc} I_m / (4\omega_s)$ (and $U_{xP}^{\max} = 4E_{xP}\omega_s / (V_{dc} I_m)$). As shown in Fig. 7, the maximum normalized energy, which means the maximum value of average capacitor voltage, decreases with injecting 2nd order harmonic circulating current. If k is 1.7, the maximum arm energy would be minimized. However the energy of the case of k=1.7 seems to be little difference that of k=1 beside increased circulating current. Hence, in this paper, the maximum k is limited to 1.

Fig. 8 shows the maximum electrical charge in the capacitor of a SM which is normalized by the magnitude of phase current. The normalized electrical charge can be calculated using numerical analysis. The normalized electrical charge is expressed as (20) which mean the maximum capacitor voltage.

$$Q_{cap}^{norm.} = C v_{cap} / I_m. \quad (20)$$

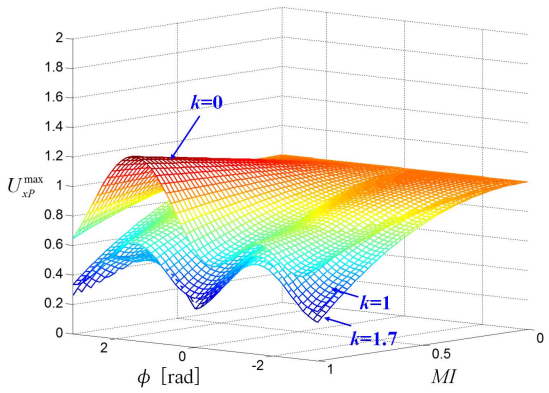


Figure 7. Maximum normalized upper arm energy with respect to the weighting factor, *k*.

With 2nd order harmonic current injection (k=1), the maximum electrical charge decreases by 26% and 33 % at $\phi = 0$ rad. and $\pi/2$ rad., respectively, as shown in Fig. 8 (a). And, in case of 100 Hz of switching frequency, the maximum electrical charge decreases by 24% and 15 % at $\phi = 0$ rad. and $\pi/2$ rad., respectively, as shown in Fig. 8 (b). Thus, the capacitor voltage fluctuation of SM can be mitigated by the harmonic circulating current in spite of the reduced switching frequency.

V. LOSS ANALYSIS

In case of half-bridge based SM, the conduction loss can be distinguished whether the arm current is positive or negative. In case of positive arm current, the conduction loss per arm, $P_{cond.}^{arm}$, can be derived as (21). In the same manner, the conduction loss can be deduced as (22) according to the sign of arm current.

$$\begin{aligned} P_{cond.}^{arm} &= \sum_{i=1}^{N} |i_{arm}| (V_{CEsat} \cdot (1 - S_k) + V_{FW} \cdot S_k) \\ &= |i_{arm}| (V_{CEsat} \sum_{i=1}^{N} (1 - S_k) + V_{FW} \sum_{i=1}^{N} S_k) \\ &= |i_{arm}| \cdot (N_{on} \cdot V_{FW} + N_{off} \cdot V_{CEsat}) \end{aligned} \quad . \tag{21}$$

where V_{FW} and V_{CEsat} represent the forward voltage of diode, and the saturation voltage of IGBT, respectively.

$$\begin{cases} P_{cond.}^{arm} = |i_{arm}| \cdot \left(N_{on} \cdot V_{FW} + N_{off} \cdot V_{CEsat} \right) & (i_{arm} \geq 0) \\ P_{cond.}^{arm} = |i_{arm}| \cdot \left(N_{off} \cdot V_{FW} + N_{on} \cdot V_{CEsat} \right) & (i_{arm} < 0) \end{cases} . \tag{22}$$

TABLE I. SWITCHING ENERGY LOSS

	S[i]	*S[i+1]*	Loss
$i_{arm} \geq 0$	0	0	*0*
		1	E_{off}
	1	0	E_{on}
		1	*0*
$i_{arm} < 0$	0	0	*0*
		1	E_{on}
	1	0	E_{off}
		1	*0*

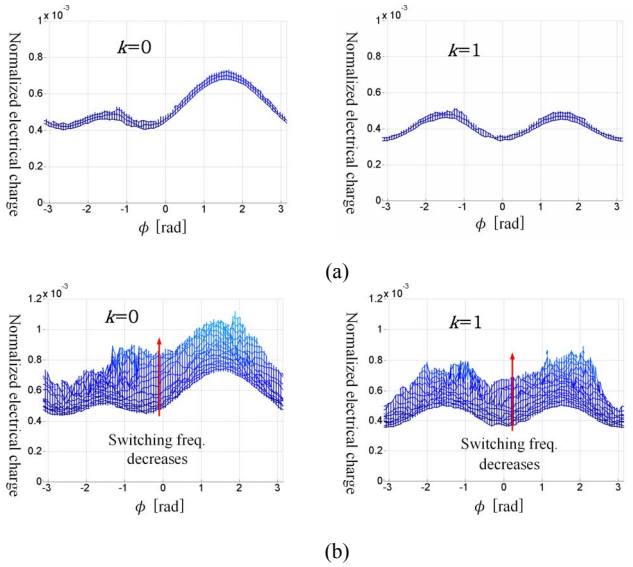


Figure 8. Maximum normalized electrical charge with respect to the weighting factor of 2nd harmonic circulating current(*MI*=0.8) (a) 500~1500 Hz of switching frequency (b) 100~500 Hz of switching frequency.

In order to analyze the switching loss of MMC, the switching energy loss is defined as (23), which is the function of capacitor voltage and arm current.

$$\begin{cases} E_{on} = f_{on}\left(v_{cap}, i_{arm}\right) \\ E_{off} = f_{off}\left(v_{cap}, i_{arm}\right) \end{cases}, \tag{23}$$

where E_{on} and E_{off} stand for the turn on energy and turn off energy, respectively. The switching loss at arbitrary sampling point can be expresses as Table. I. In Table. I, *S[i]* and *S[i+1]* represent the switching function of half-bridge circuit at i and (i+1)-th sampling point, respectively. Thus, the switching loss can be calculated as (24).

$$\begin{cases} P_{sw}^{arm} = \dfrac{1}{T_s} \displaystyle\sum_{i=1}^{T_s/T_{samp}} \sum_{k=1}^{N} \begin{pmatrix} S_k[i] \cdot E_{on}^k + S_k[i+1] \cdot E_{off}^k \\ -S_k[i] \cdot S_k[i+1] \cdot (E_{on}^k + E_{off}^k) \end{pmatrix} & (i_{arm} \geq 0) \\ P_{sw}^{arm} = \dfrac{1}{T_s} \displaystyle\sum_{i=1}^{T_s/T_{samp}} \sum_{k=1}^{N} \begin{pmatrix} S_k[i] \cdot E_{off}^k + S_k[i+1] \cdot E_{on}^k \\ -S_k[i] \cdot S_k[i+1] \cdot (E_{on}^k + E_{off}^k) \end{pmatrix} & (i_{arm} < 0) \end{cases} . \tag{24}$$

where E_{on}^k stands for the turn on energy of k-th SM, E_{off}^k stands for the turn off energy, T_s represents the fundamental period, and T_{samp} represents the sampling period. It is not simple to get the switching loss analytically because the turn on and turn off energy are the function of capacitor voltage of SM and arm current. In this paper, the switching loss has been calculated by a numerical analysis using MMC model.

VI. SIMULATION, EXPERIMENTAL RESULTS

To evaluate the performance of the proposed strategies, the computer simulation has been done using PSIM® software. The simulation condition is listed on Table II, and T2400GB45E IGBT[15] and E2400TC45C diode[16] of 4500V/2400A are used for loss analysis in this paper.

TABLE II. SIMULATTION CONDITION

Simulation parameters	Values
Grid voltage	200 kV_{rms}, 60 Hz
DC bus voltage	400 kV
Rated power	400 MVA
Number of SMs per arm	220
Nominal capacitor voltage of SM	2200 V
Capacitance of capacitor in SM	4.5 mF
Sampling frequency	10 kHz

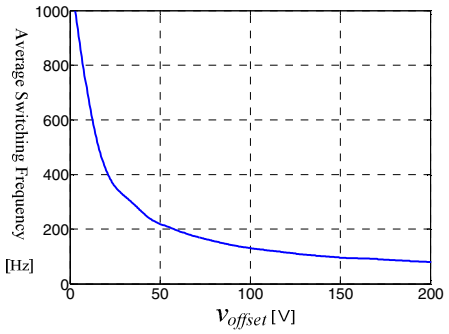


Figure 9. Average switching frequency with respect to v_{offset} ($\phi = 0$ rad.).

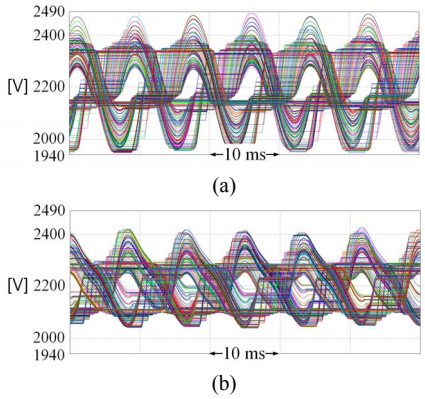


Figure 10. Capacitor voltage of 440 SM of a leg. (a) without 2nd order harmonic circulating current(k=0). (b) with 2nd order harmonic circulating current(k=1).

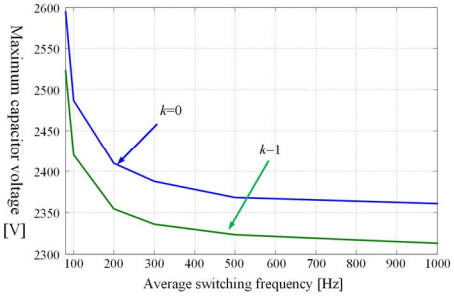


Figure 11. Maximum capacitor voltage with respect to average switching frequency.

Fig. 9 shows the simulation results of the proposed switching frequency reduction strategy. As expected from Section III, the average switching frequency decreases as v_{offset} increases. Fig. 10 shows the capacitor voltages of 440 SMs of a leg at 100 Hz of switching frequency. In addition, Fig. 11 shows

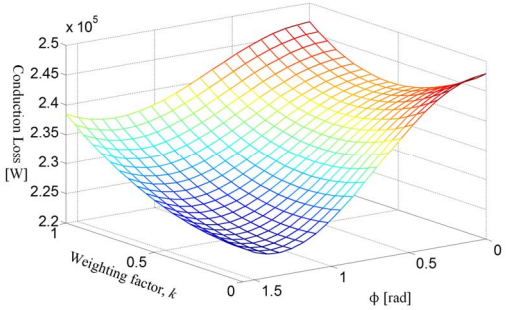


Figure 12. Conduction loss according to the variation of weighting factor, k, of 2nd order harmonic circulating current.

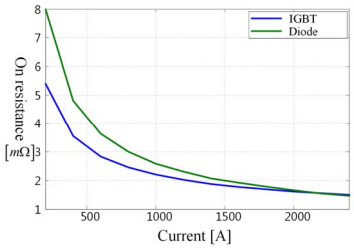


Figure 13. On resistance of IGBT and diode.

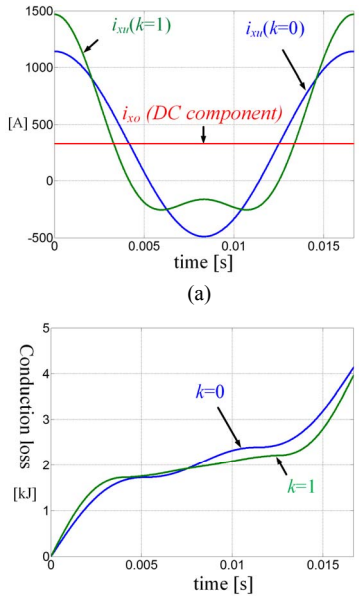


Figure 14. Conduction loss analysis. (a) waveform of arm current. (b) conduction engery loss.

the maximum capacitor voltage of SM with respect to the average switching frequency. As expected in Section IV, the voltage fluctuation is mitigated and the maximum capacitor voltage decreases with 2nd order harmonic circulating current (k=1).

Fig. 12 shows the conduction loss of one arm according to weighting factor, k, of 2nd order harmonic circulating current. The conduction loss may reduce as the 2nd order harmonic circulating current is injected because the on-resistances of IGBT and diode, which is shown in Fig. 13, are varying

according to the conduction current. It can be explained more clearly with Fig. 14. Fig. 14 (a) shows the waveform of arm current and DC component of circulating current. With 2nd order harmonic current, the maximum arm current increases and the minimum arm current decreases due to the DC component of circulating current. As shown in Fig. 14(b), the conduction loss energy with 2nd order harmonic current is smaller because the on resistance decreases as the conduction current increases.

Fig. 15 shows the total loss of one arm including the switching and conduction loss. The total loss has similar tendency whether injecting 2nd order harmonic circulating current or not, up to 420 Hz of switching frequency. It means that maximum voltage can be significantly decreased with proposed circulating current injection, achieving similar efficiency of MMC without 2nd order harmonic current injection.

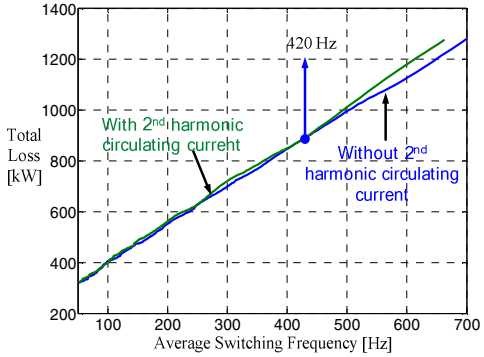


Figure 15. Total loss including switching and conduction loss ($\phi = 0$ rad.).

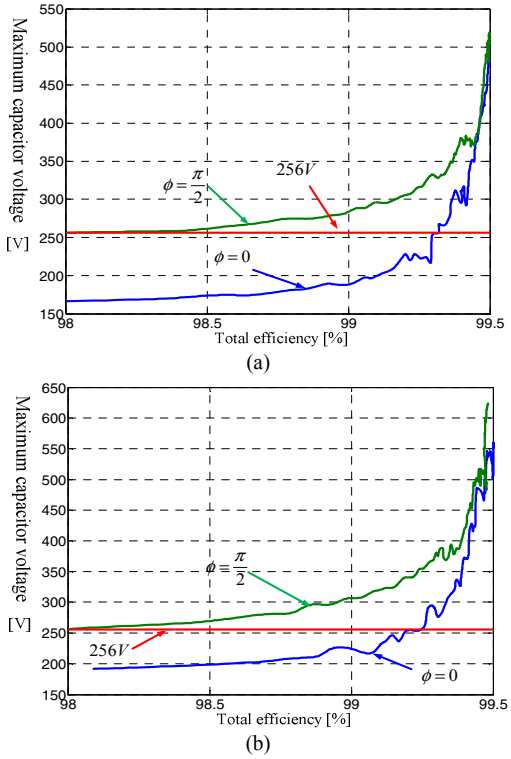


Figure 16. Maximum capacitor voltage of SM. (a) without 2nd order harmonic current in case of 4.5 mF capacitance of each SM. (b) with 2nd order harmonic current in case of 3 mF capacitance of each SM.

TABLE III. EXPERIMENT CONDITION

Simulation parameters	Values
Grid voltage	110 V_{rms}, 60 Hz
DC voltage	200 V
Sampling frequency	10 kHz
Number of SMs per arm	6
Nominal capacitor voltage of SM	40 V
Capacitance of capacitor in SM	4.4 mF
Arm inductance	2 mH
Rated power	6 kW

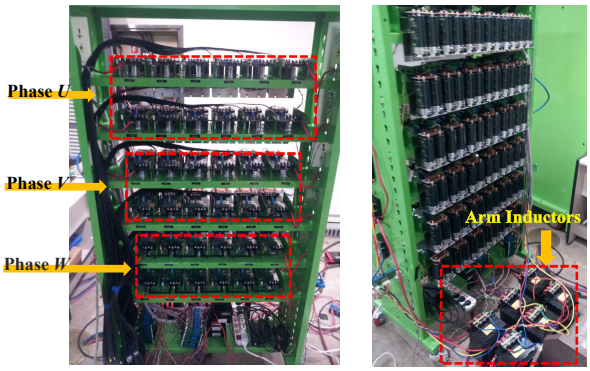


Figure 17. Prototype 7-level MMC.

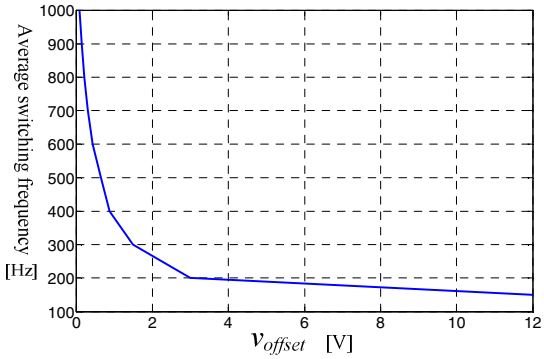
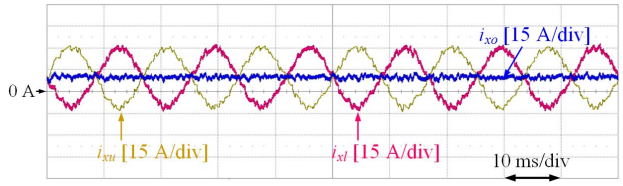


Figure 18. Average switching frequency with respect to v_{offset}.

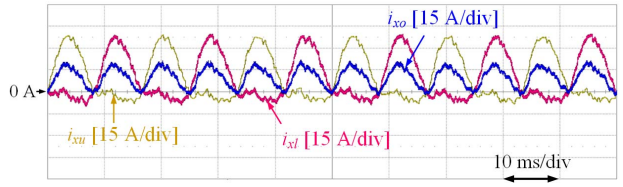
Fig. 16 shows the maximum capacitor voltage of SM with respect to overall efficiency of MMC. It is assumed that the worst case of operating condition is $\phi = \pi / 2$ rad. where the capacitor has the maximum voltage. As shown Fig. 16 (a), without 2nd order harmonic current, '4.5 mF' of SM capacitor has the operation efficiency of 99.3% allowing maximum voltage with about 10 % of nominal capacitor voltage. However, with 2nd order harmonic current, '3 mF' of SM capacitor has the operation efficiency of 99.25% allowing same maximum voltage which is shown in Fig. 16 (b). It can be noted that the capacitance of SM capacitor can be reduced by 33% while MMC has the efficiency degradation of only 0.05 % in the given simulation condition.

Series of experiments were performed to verify the feasibility of proposed strategies. The experimental condition is listed on Table III. Fig. 17 shows the prototype 7-level MMC for experimental setup. Fig. 18 shows the experimental results for proposed switching frequency reduction strategy under the modulation index and ϕ are 0.9172, 0.166 rad., respectively. As expected in Section III, the average switching frequency

decreases to 150 Hz as v_{offset} increases. Fig. 19 shows the upper arm, lower arm, and circulating current according to the 2nd order harmonic circulating current injection at rated power. Fig. 20 shows the capacitor voltage of 4 SM at 150 Hz of average switching frequency, and Fig. 21 shows the maximum capacitor voltage with respect to the average switching frequency. As expected from Section IV, the maximum capacitor voltage decreases with the 2nd order harmonic circulating current.

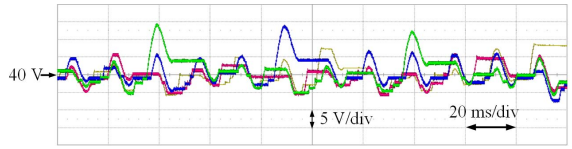


(a)

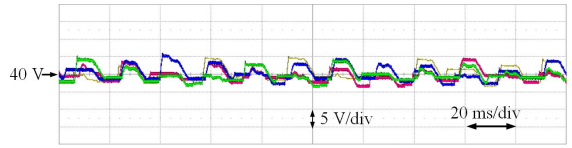


(b)

Figure 19. Waveform of arm current and circulating current. (a) without 2nd harmonic circulating current. (b) with 2nd harmonic circulating current.



(a)



(b)

Figure 20. Capacitor voltage of 4 SM at 150 Hz of switching frequency (a) without 2nd harmonic circulating current. (b) with 2nd harmonic circulating current.

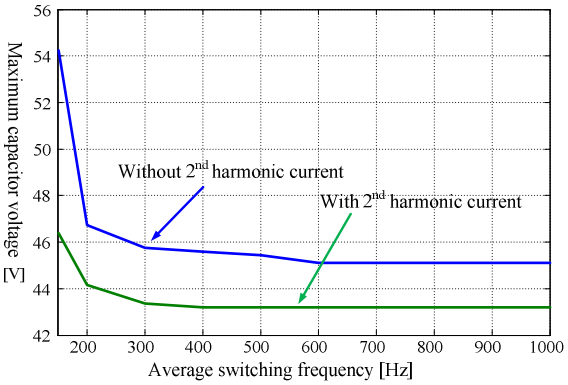


Figure 21. Maximum capacitor voltage with respect to average switching frequency.

VII. Conclusion

In this paper, a novel switching frequency reduction strategy for MMC has been proposed using the sorting method with a virtual capacitor voltage of individual SMs. The voltage fluctuation of capacitor in SM, however, increases as the switching frequency decreases. Hence, this paper presents the 2nd order harmonic circulating current injection to mitigate the voltage fluctuation. To evaluate the effectiveness of the proposed strategies, the computer simulation with 400 kV, 400 MVA, 221-level MMC has been performed. With these strategies, it is identified that the capacitance of SM capacitor could be reduced by 33% at the cost of only 0.05 % efficiency degradation in the given simulation condition. Additionally, validity of the proposed strategies has been verified by 200 V, 7-level down scaled prototype experimental setup.

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