Principle, Control and Comparison of Modular Multilevel Converters (MMCs) with DC Short Circuit Fault Ride-through Capability

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***Abstract*—Lack of DC short circuit fault blocking and ride through capability is one of main issues in applications of Modular Multilevel Converter (MMC) to actual HVDC transmission system. Recently, several topologies have been proposed to provide DC short circuit fault blocking capability and/or DC fault ride through capability. In this paper, the operation principles, functionalities, and characteristics of several topologies are compared. And, it's revealed that the conventional leg capacitor energy balancing strategy by regulating DC component of leg current fails under DC short circuit fault. A corresponding new leg capacitor energy balancing method by common mode voltage injection is proposed. Validity of the proposed method is verified by computer simulation.**

I. INTRODUCTION

A High Voltage Direct Current (HVDC) transmission is a key technology for the future large scale smart grid which integrates a great amount of renewable energy sources [1-3]. Compared to two/three level VSC-based HVDC system, MMC-based HVDC shown in Fig.1 presents many merits such as remarkably reduced size of filters, low dv/dt, modularity and simple scaling, free of IGBT series operation, much lower switching loss, elimination of DC bus capacitor [4-9]. Since a high power DC breaker is not fully demonstrated and extremely expensive, the employment of the DC breaker in HVDC transmission is still far from wide acceptance. At the moment, how to deal with the DC short circuit fault is one of main issues for VSC-based HVDC transmission system.

When a DC short circuit fault happens, the active power of AC side of MMC is not able to be transferred into DC bus. Then, MMC should not only prevent the DC short circuit fault from extending to the AC side of MMC, but also clear the DC fault current. If the MMC can control the DC fault current to be null at the cost of losing the AC current control ability, then this is called as DC short circuit fault blocking capability in this paper. In this case, AC grid should be decoupled though the AC circuit breaker. While, if the MMC can not only control the DC fault current to be null with the control capability of AC grid side reactive power, then this is called as DC short circuit fault ride through capability. The MMC which has the DC short circuit fault ride-through capability can work as a STATCOM during DC short circuit fault condition to support AC grid.

Simplified schematic of a MMC-based HVDC transmission system is shown in Fig. 1. A MMC consists of three legs for three phases, and each leg consists of an upper arm and a lower arm. Each arm usually contains numerous (up to several hundreds) sub-modules and sub-modules can be constructed in different topologies. To provide DC short circuit fault blocking or ride-through capability, numerous efforts had been done. For the conventional half-bridge based MMC which had been commercialized in Transbay project by Siemens® [10], increasing arm inductance is a normal way to

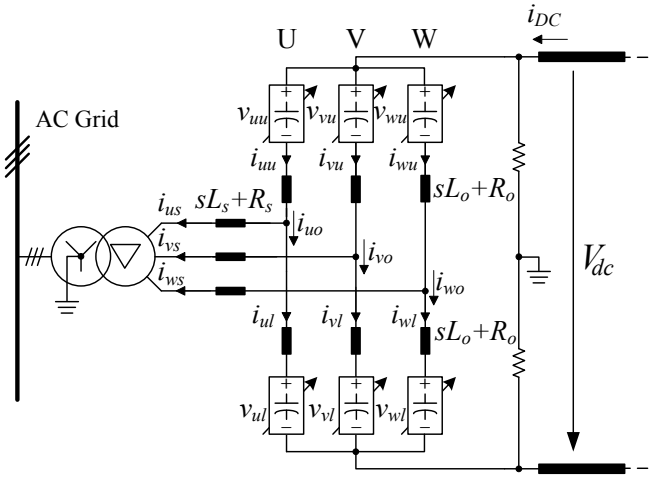


Figure 1. Simplified schematic of a MMC-based HVDC transmission system.

limit over-current before blocking the converter. And high current capacity bypass thyristors were employed to protect IGBT modules after blocking the converter. Otherwise, a full-bridge sub-module based MMC had been presented since it can operate like a STATCOM when DC short circuit fault occurs and ride through the fault. Even though it's easy for realization, it suffers from large number of IGBTs and higher conduction loss. In [11], a new MMC sub-module named clamp double sub-module employing an auxiliary IGBT and two diodes was proposed. It's capable to block fault current when a DC short circuit fault occurs and no auxiliary bypass thyristor is needed. However, because of the deficiency of DC fault ride-through capability, it cannot operate as a STATCOM to support the AC grids during fault. In [12], a new hybrid MMC topology with DC fault ride through capability was proposed. Its number of full-bridge sub-modules is only half the number of the conventional MMC, and its conducting loss is theoretically lower than the conventional half-bridge based MMC. However, it calls for series operation of IGBTs as a static AC switch. Since, at the moment, IGBT series operation is still a difficult issue because of several penalties such as snubber circuit, complex gate control logic, and increased switching loss, it will not be discussed in this paper. Recently, a new half-bridge and full-bridge hybrid MMC topology was proposed in [13]. This topology provided DC short circuit fault ride-through capability with less cost of increased IGBTs and conduction loss compared to the full-bridge based topology and seems to be a very promising solution for DC short circuit fault management.

In Section II, principles of existed topologies for DC short circuit fault blocking and/or ride through are introduced and reviewed. In Section III, these different topologies are compared and contrasted. In Section IV, a novel leg capacitor energy balancing strategy is proposed for DC short circuit fault ride through and validity of the proposed strategy is verified in Section V by computer simulation.

II. Principles of MMC Topologies for DC Short Circuit Fault Blocking and Ride Through

A. *Principle of conventional half-bridge chopper based MMC*

The conventional MMC is based on half-bridge choppers. As shown in Fig. 2, each sub-module has a bypass thyristor. When a DC short circuit fault occurs, due to diode free-wheeling effect, the bypass thyristor should be fired synchronously with the diode. Thus during DC short circuit fault, the MMC operates like a three phase diode rectifier as shown in Fig. 2(a) and a inrush current flows in both AC and DC sides. Magnitude of the inrush AC and DC side currents during fault can only be limited by increasing inductances of arm inductors. In [14], it's revealed that if inductance of arm inductor is 0.24 p.u., then peak currents flow through thyristor and parallel diode in IGBT module can reach up to 4 p.u. and 2 p.u. respectively. For this sub-module protection scheme, DC transmission line fault current cannot be cleared unless AC grid is disconnected by an high speed AC circuit breaker.

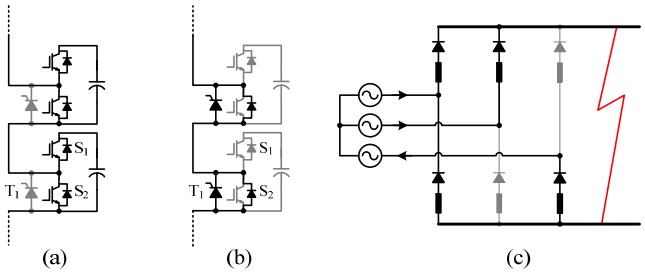


Figure 2. Principles of the conventional MMC based on conventional half-bridge sub-modules. (a) Operation of an arm during normal operation. (b) Operation of an arm during DC short circuit fault. (c) Equivalent MMC circuit during DC short circuit fault.

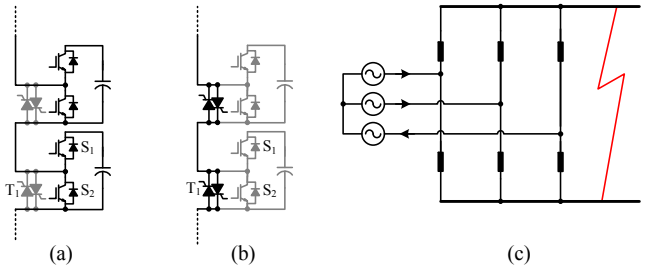


Figure 3. Principles of a MMC for protection of nonpermanent faults. (a) Operation of an arm during normal operation. (b) Operation of an arm during Dc short circuit fault. (c) Equivalent circuit during DC short circuit.

A new protection scheme for nonpermanent faults is proposed in [14]. In this scheme, each sub-module is bypassed by a bidirectional switch consists of double thyristors during DC short circuit fault. By employing this scheme, operation restriction due to diode free-wheeling can be eliminated and DC transmission line current decays in hundreds of mili-seconds. Then for nonpermanent DC short circuit fault such as overhead line short circuit caused by lightning strike, the DC arc can be extinguished and normal operation can be recovered.

Regardless of sub-module protection scheme, the conventional half-bridge based MMC cannot block fault current and a considerable inrush current can flows through parallel diodes in IGBT modules. In addition, the conventional topology is not able to ride through DC short circuit fault.

B. *Principle of full-bridge chopper based MMC*

Even though a full-bridge chopper can be modulated in bipolar or unipolar mode, to minimize switching loss, one of the lower switch should be normally on and the other corresponding complementary switch should be normally off during normal operation as shown in Fig. 4(a). Then during normal operation, the full-bridge chopper based MMC operates like a conventional half-bridge chopper based MMC.

When a DC short circuit fault occurs, each sub-module operates like a normal full-bridge and the DC bus voltage is synthesized as zero to clear DC transmission line short circuit current. Since a full-bridge chopper can output bipolar voltage, the converter can generate back-EMF to regulate AC side current during fault.

C. Principle of hybrid full-bridge and half-bridge chopper based MMC

It should be noted that the full-bridge based MMC can output back-EMF to regulate AC side current while the DC bus is synthesized from $-V_{dc}$ to $+V_{dc}$. When the MMC operates at normal mode, the DC bus voltage should be synthesized as $+V_{dc}$, and when a DC short circuit fault occurs the DC bus voltage should be synthesized as 0. Then in fact half of the DC bus voltage output capability is redundant. Using a half-bridge and full-bridge hybrid structure can take full advantage of converter output voltage capability. As shown in Fig. 4(c), during normal condition the hybrid converter operates like a conventional MMC, and during DC short circuit fault the half-bridge choppers are bypassed and the converter operates like a full-bridge based MMC to ride through the fault.

D. Principle of clamp double sub-module based MMC

During normal operation, the auxiliary clamping switch T_a is switched on and then auxiliary clamping diodes D_a and D_b are reverse blocked as shown in Fig. 5(a). Then the converter is topologically equal to the conventional MMC. When a DC short circuit fault occurs, the switch T_a is switched off. When current i is positive, then current flows through clamping diodes D_a and D_b. Otherwise, current flows through the free-wheeling diode in T_a. Since current flows through clamping diodes during fault, polarity of sub-module output voltage is affected by current direction. Then even though it can nullify the DC bus voltage to eliminate DC transmission line current and generate back-EMF in AC side to block AC grid inrush current, it is lack of ability to ride through the DC short circuit fault as a STATCOM to support AC grid.

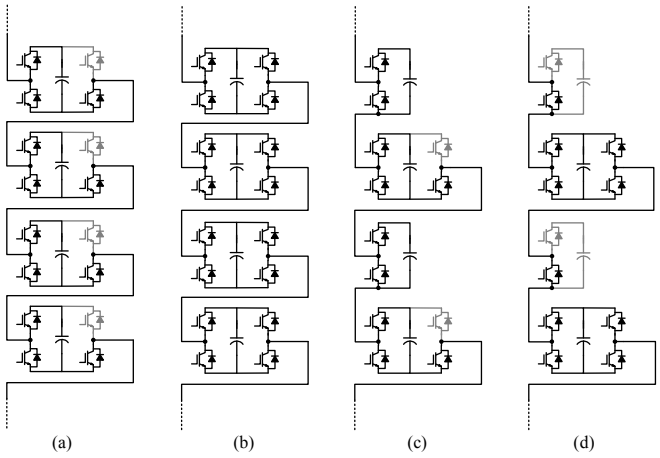


Figure 4. (a) Operation of an arm in full-bridge based MMC during normal operation. (b) Operation of an arm in full-bridge based MMC during DC short circuit fault. (c) Operation of an arm in hybrid half-bridge and full-bridge based MMC during normal operation. (d) Operation of an arm in hybrid half-bridge and full-bridge based MMC during DC short circuit fault.

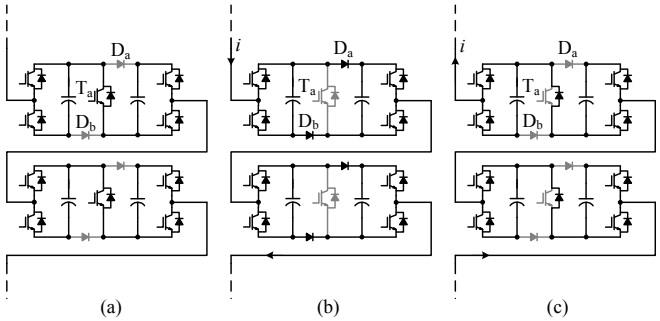


Figure 5. (a) Operation of an arm in clamp double sub-module based MMC during normal operation. (b) and (c) Operation of an arm in clamp double sub-module based MMC during DC short circuit fault when $i>0$ and $i<0$ respectively.

III. Comparison and Contrast of Operation Principles and Characteristics

A detailed comparison of the topologies introduced in Section II is given in TABLE. I. Compared to the classical half-bridge based MMC, the hybrid topology in [12] employs 50% more IGBT modules. Nevertheless, high current bypass protection thyristors can be saved. Conduction loss of the hybrid one in the normal operation may be approximately 50% higher than that of the conventional half bridge based MMC. Compared to the full-bridge based MMC, the topology in [12] only employs 75% IGBT modules and saves approximately 25% conduction loss but gains the same DC fault blocking and ride through functionalities. Compared to the clamp double sub-module topology proposed in [10], the hybrid topology employs 20% more IGBT modules but the clamping diodes are eliminated. Conduction losses of the hybrid half-bridge and full-bridge based converter and that of the clamp double sub-module based converter would be almost equal. But it should be noticed that the clamp double sub-module based one is not capable for DC short circuit fault ride-through.

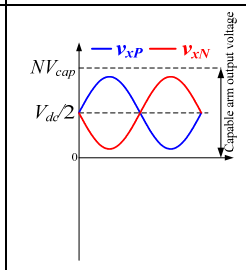
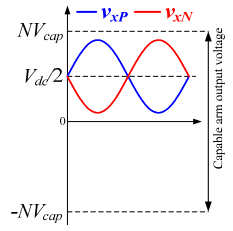
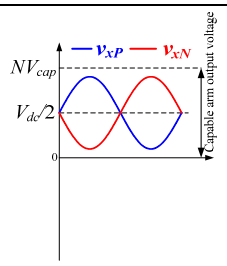
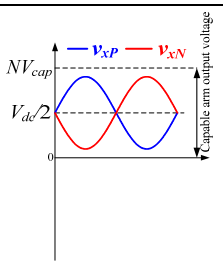
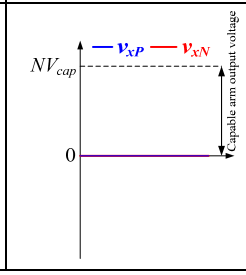
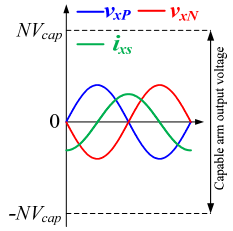
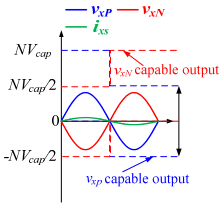
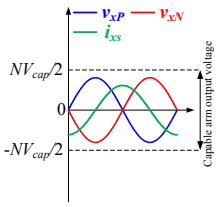
In summary, compared to the full-bridge based MMC or clamp double sub-module based MMC in [10], the hybrid topology provides DC fault blocking and ride through capabilities with almost same or lower cost and less conduction loss. When compared with classical half-bridge based MMC, the proposed one calls for more IGBT modules (but no bypass protection thyristors) and leads to higher conduction loss. Considering that today's power semiconductor price tendency (power semiconductor price is around only 15% of total investment in a MMC HVDC system), the half-bridge and full-bridge hybrid topology is a very promising solution to deal with DC short circuit fault.

IV. MMC Control during DC Short Circuit Fault

Modeling of the DC side of a MMC is shown in Fig.6 (a) [15]. DC short circuit fault occurs at $t=t_f$ as in Fig.6(b). For the worst case, DC bus line impedance L_{dc}, R_{dc} is almost zero and at sampling instant $t=t_1$, instantaneous DC current is a little lower than the DC short circuit fault detection threshold. At next sampling instant $t=t_2$, DC short circuit fault is detected. Then at the following sampling instant $t=t_3$, DC bus voltage is modulated to zero instantaneously to suppress DC side inrush current.

In Fig.1, a simplified schematic of a MMC in HVDC is shown, where an arm can be regarded as a variable voltage source to control the MMC. If the phase number is denoted as x ($x=u, v, w$), then following equations can be deduced [16].

TABLE I. COMPARISON BETWEEN DIFFERENT MMC TOPOLOGIES

	Conventional half-bridge based MMC	Full-bridge based MMC	Topology proposed in [10]	Topology proposed in [12]
Cell per arm	N	N	N	N
IGBT per arm	2*N	4*N	2.5*N	3*N
DC short circuit fault blocking	No	Yes	Yes	Yes
DC short circuit fault ride through as a STATCOM	No	Yes	No	Yes
Conducting IGBTs per leg	2*N	4*N	3*N	3*N
Conduction Loss	Low	High	Medium	Medium
Bypass Thyristors	Necessary	Not required	Not required	Not required
Principle in normal operation (Arm voltage reference)				
Principle under DC short circuit fault (Arm voltage reference)				

$$-\frac{v_{xu}-v_{xl}}{2}-v_{xg}=v_{xs}-v_{xg}=\{(\frac{R_o}{2}+R_s)+(\frac{L_o}{2}+L_s)\frac{d}{dt}\}i_{xs}. \quad (1)$$

$$V_{dc}-(v_{xu}+v_{xl})=2v_{xo}=2(R_o+L_o\frac{d}{dt})i_{xo}. \quad (2)$$

$$i_{xo}=\frac{i_{xu}+i_{xl}}{2}. \quad (3)$$

From (1)-(2), output voltage v_{xs} can be used to regulate the AC current, and the leg current i_{xo} , which is defined in (3), can be regulated by v_{xo} (v_{xo} is named leg internal voltage in this paper). Then to generate desired output voltage v_{xs} and leg internal voltage v_{xo}, upper and lower arm output voltages in Fig. 1 should be synthesized as (4) and (5) respectively.

$$v_{xu}^*=\frac{V_{dc}^*}{2}-v_{xs}^*-v_{xo}^*. \quad (4)$$

$$v_{xl}^*=\frac{V_{dc}^*}{2}+v_{xs}^*-v_{xo}^*. \quad (5)$$

And, the upper and lower arm current can be written as (6) and (7).

$$i_{xu}=\frac{1}{2}i_{xs}+i_{xo}. \quad (6)$$

$$i_{xl}=-\frac{1}{2}i_{xs}+i_{xo}. \quad (7)$$

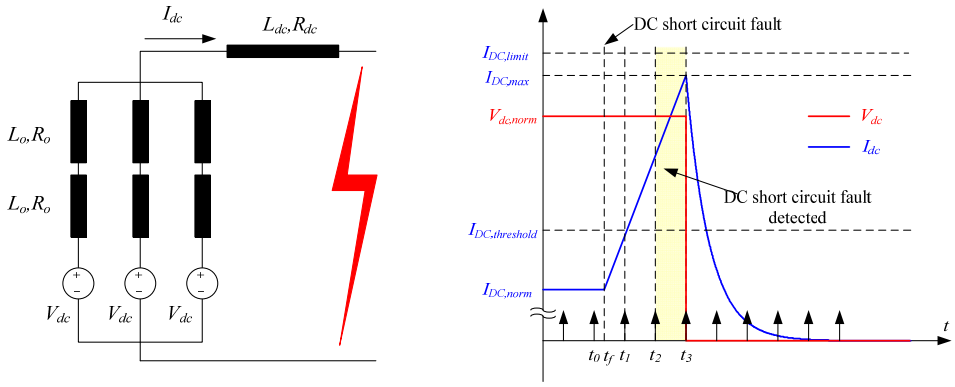
To balance the arm capacitor energy, the power flow into a leg should be considered. Power that flows into upper and lower arms in the same leg is calculated as (8) and (9), respectively.

$$P_{xu}=\frac{dE_{xu}}{dt}=v_{xu}^*i_{xu}=(\frac{V_{dc}^*}{2}-v_{xs}^*-v_{xo}^*)(i_{xo}+\frac{1}{2}i_{xs}). \quad (8)$$

$$P_{xl}=\frac{dE_{xl}}{dt}=v_{xl}^*i_{xl}=(\frac{V_{dc}^*}{2}+v_{xs}^*-v_{xo}^*)(i_{xo}-\frac{1}{2}i_{xs}). \quad (9)$$

Then sum and difference of power that flows into upper and lower arms in the same leg are calculated as (10) and (11).

$$P_x^{\Sigma}=P_{xu}+P_{xl}=\frac{dE_x^{\Sigma}}{dt}=V_{dc}i_{xo}-v_{xs}^*i_{xs}-2v_{xo}^*i_{xo}. \quad (10)$$



(a) (b)

Figure 6. Transient of DC current under DC short circuit fault. (a) Modeling of the DC side of a MMC in DC side. (b) Transient waveforms of DC voltage and current when DC short circuit fault occurs.

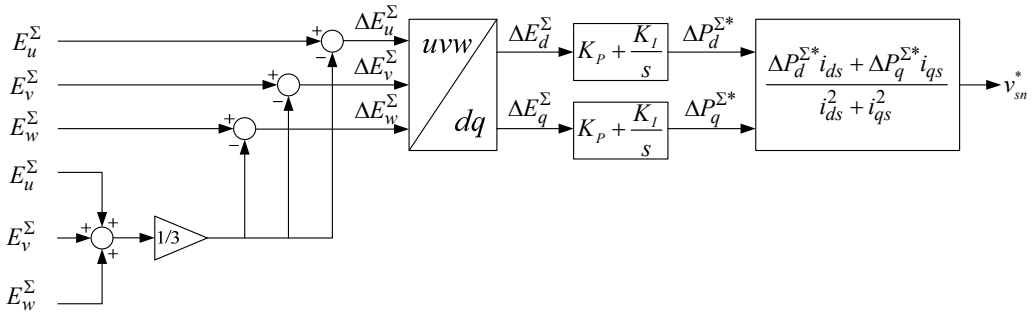


Figure 7. Block diagram of the proposed leg capacitor energy balancing strategy during DC short circuit fault.

$$P_x^\Delta = P_{xu} - P_{xl} = \frac{dE_x^\Delta}{dt} = \frac{1}{2}V_{dc}i_{xs} - 2v_{xs}^* i_{xo} - v_{xo}^* i_{xs}. \quad (11)$$

Generally, the energy balance among six arms can be achieved through (10) and (11). In normal operation, leg capacitor energy was balanced by regulating the DC component of the leg current i_{xo} in the conventional control strategy, namely by controlling the first term in the right side of (10). However, when a DC short circuit fault occurs, V_{dc}^* drops to zero to clear DC transmission line current and then the leg current cannot balance the leg capacitor energy between three phases since the first term in the right side of (10) is always null. In this paper, a leg capacitor energy balancing strategy using common mode voltage v_{sn} during DC short circuit fault is proposed as shown in Fig. 7. The common mode voltage and the AC current can be described as (12) and (13).

$$v_{sn}^* = V_{cm}\sin(\omega t + \alpha). \quad (12)$$

$$\begin{cases} i_{us} = I_s \sin(\omega t + \varphi). \\ i_{vs} = I_s \sin(\omega t + \varphi - \frac{2}{3}\pi). \\ i_{ws} = I_s \sin(\omega t + \varphi + \frac{2}{3}\pi). \end{cases} \quad (13)$$

If the common mode voltage is considered in the arm power equation, the leg power of three phases caused by injected common mode voltage can be calculated as (14), which can be converted into d-q axis as (15)

$$\begin{cases} \bar{P}_u^\Sigma = \frac{1}{2}V_{cm}I_s\cos(\varphi-\alpha). \\ \bar{P}_v^\Sigma = \frac{1}{2}V_{cm}I_s\cos(\varphi-\alpha-\frac{2}{3}\pi). \\ \bar{P}_w^\Sigma = \frac{1}{2}V_{cm}I_s\cos(\varphi-\alpha+\frac{2}{3}\pi). \end{cases} \quad (14)$$

$$\begin{cases} P_d^\Sigma = \frac{1}{2}V_{cm}I_s\cos(\varphi-\alpha). \\ P_q^\Sigma = \frac{1}{2}V_{cm}I_s\sin(\varphi-\alpha). \end{cases} \quad (15)$$

According to (15), three phase leg energy can be balanced by adjusting the magnitude and the phase of the injected common mode voltage. In accordance with (12)-(15), reference value of the common mode voltage injection can be calculated as (16),

$$v_{sn}^* = \mathrm{Re}\left\{\frac{P_d^{\Sigma*} + jP_q^{\Sigma*}}{\frac{1}{2}(i_{ds}+ji_{qs})}\right\} \quad (16)$$

where "Re{ }" stands for real part of { }.

V. Verification of Proposed Leg Capacitor Energy Balancing Strategy

A full-scale version point-to-point HVDC transmission system based on half-bridge and full-bridge hybrid MMCs with 217 levels is simulated by PSIM®. The parameters for the computer simulation are given in Table II. The DC transmission line is emulated as an inductor.

Scenario of the simulation is as following. The MMC-I and MMC-II import reactive power into Grid I and Grid II independently. The command of active power that flows from MMC-I to MMC-II increases from 0 to 400MW during t=1.0~1.25s. Then power flow starts to reverse from 400MW to -400MW during t=1.75~2.0s. During t=2.0~2.8s, a short circuit fault occurs in on point in transmission line as shown in Fig. 8. Threshold value of DC transmission line current for DC short circuit fault detection is set as 2kA. As soon as the DC short circuit fault is detected, the protection scheme is activated and the DC bus output voltages of MMC-I and MMC-II is nullified and the current of DC transmission line decays to zero. After the short circuit fault is cleared, the transmission system restarts and the power flow from MMC-II to MMC-I starts to increase from 0 to 400MW since t=3.0s.

As shown in Fig. 9, when a DC short circuit fault occurred at t=2.0s, both MMCs detected fault and modulated DC bus output voltages V_{dc} to zero instantaneously. Then DC side short circuit current was suppressed to null. Because the DC transmission line was not transmitting any power during fault, AC side active power of both MMC-I and MMC-II became zero. However the reactive power was controlled independently for each MMC as like STATCOM did during DC short circuit fault and both converters rode through the fault period. As shown in Fig. 10, after the MMC detected DC short circuit fault and protection scheme was activated, half-bridge sub-modules were bypassed and no fluctuation appeared in voltages of half-bridge sub-module capacitors.

In Fig. 11, leg capacitor energy when using the conventional and the proposed leg capacitor energy balancing strategy is presented. It can be observed that during DC short circuit fault ride through period, since the DC bus voltage became null, the conventional balancing strategy cannot balance leg capacitor energy. However, the proposed leg capacitor energy balancing strategy by injecting common mode voltage can balance leg capacitor energy well to ride through the DC short circuit fault. It should be noticed that leg energy reference becomes a half value since half number of sub-modules (half bridges) are bypassed and only the other half sub-modules (full bridges) are employed during DC short circuit fault.

VI. Conclusion

To manage the DC short circuit fault in VSC-HVDC transmission system based on MMC, several topologies of MMC had been proposed for DC short circuit fault blocking and/or ride-through. Their operation principles and characteristics have been compared and contrasted in this paper. A half-bridge and full-bridge hybrid MMC topology is considered as a promising solution considering its both advantages and disadvantages. It's revealed in this paper that the conventional leg capacitor energy balancing strategy by injecting DC component in leg current is not valid during DC short circuit fault, and an effective balancing strategy by injecting common mode voltage has been proposed for balancing the leg capacitor energy. DC short circuit fault ride capability of the hybrid MMC topology has been studied by computer simulation. Validity of the proposed leg capacitor energy control strategy during fault ride through has been confirmed by the simulation.

TABLE II. Simulation Parameters

Quantity	Values
Number of half-bridge sub-modules per arm	108
Number of full-bridge sub-modules per arm	108
Rated DC bus voltage (V_{dc}^{*})	±200 kV
Rated cell capacitor voltage (V_{cell}^{*})	2.2 kV
Cell capacitor (C_{cell})	4.5 mF
Grid line-to-line voltage (RMS)	180.2 kV
Arm inductor inductance (L_o)	15.0 mH
Arm inductor resistance (R_o)	367.0 mΩ
Sampling frequency (f_{samp})	10.0 kHz
Transmission line inductance ($L_{dc,I}$)	30.0 mH
Transmission line inductance ($L_{dc,II}$)	20.0 mH

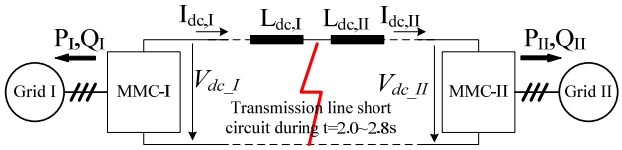


Figure 8. Conceptual diagram of simulation.

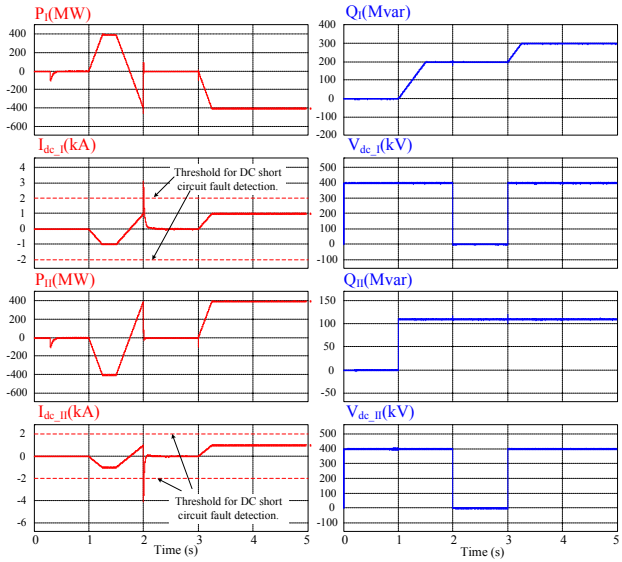


Figure 9. Active power, reactive power, DC bus voltage, and DC transmission line current of MMCs.

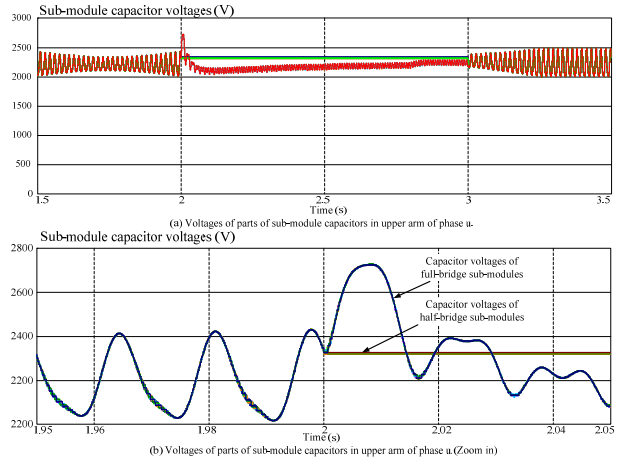


Figure 10. Voltages of parts of sub-module capacitors in upper arm of phase u.

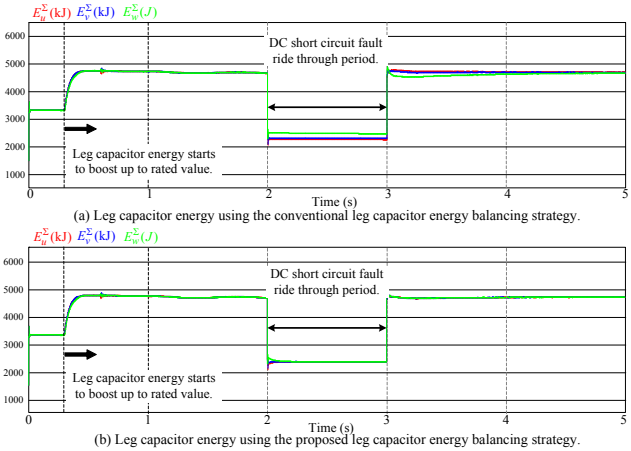


Figure 11. Leg capacitor energy using the conventional and the proposed leg capacitor energy balancing strategy.

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