Reduced Sampling Rate for Cell Voltage Sensing in High-level Modular Multilevel Converter

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Abstract—**This paper presents an estimation scheme of cell capacitor voltage for the Modular Multilevel Converter (MMC) to reduce the sampling data and its associated communication time coming from enormous number of cells in HVDC application. For the control of cell capacitor voltage of each cell, it is necessary to know the state of the voltage and it is generally measured by voltage sensors. And, to sample the voltage of each cell at every sampling instant, the associated measurement and communication hardware and signal processing time would be prohibitive as the number of cells in each arm of MMC for HVDC application is above several hundreds. This paper presents an estimation of the cell capacitor voltages using sub-module grouping and adaptive observer for estimating cell capacitance in order to reduce real time voltage measurement burdens. The simulation and experimental results verify that the proposed method can guarantees the stable operation of MMC with reduced number of the cell voltage sampling.**

Keywords—Modular Multilvel Converter; sensor reduction; cost reduction; sampling; cell voltage sensing

I. INTRODUCTION

Nowadays, the demand of higher power applications has increased considerably. Multilevel converters have emerged as an attractive technology in comparison to their two level counterparts, not only for the higher number of output voltage steps but also for better power quality than them [1]-[3]. Among the multilevel converters, a modular multilevel converter (MMC) has attracted significant attention. These converters can be composed of numerous identical sub-module cells. Every cell contains two active switching devices and one capacitor in the case of half-bridge circuit based cells. Because the number of the output voltage levels depends on the number of cell, it is easy to increase the amount of levels by adding more cells. A voltage balancing strategy should be carried out for the stable operation of MMC [3]-[5]. In order to ensure the proper voltage balancing strategy, it is necessary to acquire accurate voltage data of each cell at every sampling instant. Therefore, a control system for MMC requires sampling for hundreds or even thousands of cell voltages at every sampling instant. This heavy sampling at once has the adverse effects on analog-to-digital conversion (ADC) and communication bottleneck under the assumption that no special techniques are applied. If it is assumed that the main control system measures all of the cell voltages, the implementation burden can be drastically increased because of a parallel connection between the main control system and all of the cells. A serial communication scheme can be employed to reduce the implementation burden. However, even in the modern fast communication system the communication period might be increased and the sampled data would be too much delayed due to the huge data from thousands of the cells. And, the sampling frequency could be constrained by the communication bottleneck. In the result, the control performance would be deteriorated and the voltage ripple of cell capacitor would increase with the reduced sampling frequency. In this paper an estimation scheme of cell voltage is proposed to reduce the cost of handling enormous sampling data. The cells in system are divided into several groups, and processor samples one group's voltages at one sampling instant. Consequently, it makes the sampling burden of processor conspicuously be small. To do that, the cell capacitance should be estimated in on-line. In this paper, an adaptive estimation scheme is employed. The adaptive estimator is the control method which is adapted to the system with parameters which may vary, or are initially uncertain. Finally, time-domain simulation results with a high-level MMC obtained by PSIM software and some experimental tests with scaled version of MMC have been performed to verify the effectiveness of the devised method.

II. SYSTEM CONFIGURATION

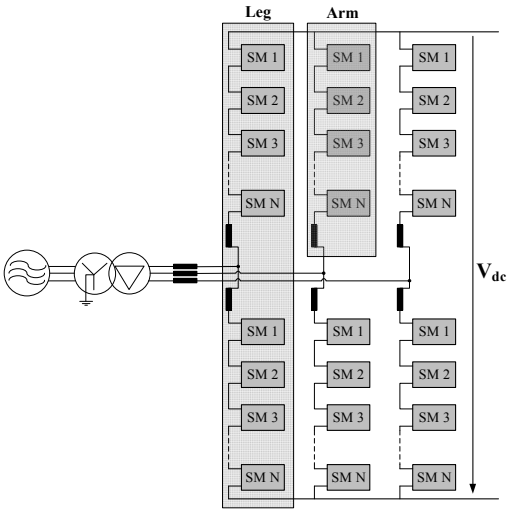

Figure 1. Simplified circuit configuration of an MMC.

The circuit configuration of an MMC is shown as Fig. 1. The three-phase MMC is composed of three legs, and each leg has upper and lower arms and two arm inductors. Each arm has cascaded N-identical cells. And each cell consists of one DC storage capacitor and two active switching devices in case of half-bridge based cells. The sub-module can also be full-bridge based cell.

An arm can be regarded as a voltage source. The ON-state of sub-module cell means that the output voltage of cell equals the capacitor voltage. And, the OFF-state means that the output voltage of cell is zero. In the ON-state, the charging or discharging of the cell capacitor depends on the relationship between the arm current direction and the switching state of cell. In the OFF-state, in contrast, the capacitor voltage is constant, irrespective of the arm current direction. Because of the flow of the output current, the cell capacitor voltage fluctuates with the fundamental output phase frequency [8]. Therefore, the cell capacitor balancing control is very important. The measurement of the cell capacitor voltage is prerequisite for the cell voltage balancing.

III. Proposed Scheme for Reducing Sampling Rates

In general, an MMC with N sub-modules per one arm requires 6N triangular carriers in totally. In the phase-shifted carrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves of sub-module cells in one arm, given by $2\pi / N$. In the phase-shifted carrier PWM, the arm voltage is produced by the sum of each cell output voltage, and each cell voltage reference is same assuming that the cell voltages are balanced. The balancing schemes in the phase-shifted carrier PWM are addressed in [11]-[12]. The magnitude of the arm current that flows through the cell capacitor is the same through all sub-module cells. To keep the cell capacitor voltage from diverging, a cell voltage controller is separately needed for every cell. Therefore, as the number of cells increases, the burden of cell capacitor voltage controller can increase. And, due to the inherent characteristic of the phase-shifted PWM with an MMC, the switching loss and the output voltage distortion can be larger, compared with the level-shifted PWM as analyzed in [11].

In the level-shifted PWM, on the other hand, it requires N triangular carriers, all having the same frequency and amplitude. The N triangular carriers are vertically disposed such that the bands they occupy are contiguous. The level-shifted PWM can be divided into three types: Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative POD. For simplicity, this paper focuses on PD-PWM where all carriers are in phase since it provides the best harmonic profile among three types [9]-[10]. In PD-PWM, the switching frequency is not the same for the devices in different sub-module cells. Since the ON duties applied to each cell are not the same, the cell capacitor voltages may be unbalanced. The balancing schemes should be needed, and one of the typical and simple cell balancing methods is the sorting algorithm. The capacitor voltages after measuring are sorted out in the descending or ascending order. If the arm current direction is positive, the sub-modules with lower DC voltage are selected and inserted to be charged. If the arm current has negative direction, the sub-modules with higher DC voltage are selected and inserted to be discharged. Because the level-shifted PWM is easy to be implemented, it is appropriate for high level MMC control. Therefore, this paper will propose a method for reducing sampling rates of the measurement of cell voltage, under the assumption that the level-shifted PWM is adopted for modulation of the MMC.

A. Grouping of Sub-module Cells

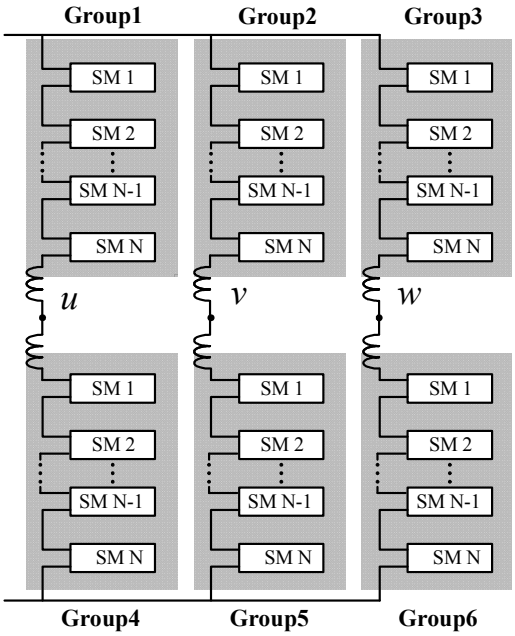

Figure 2. Six sensing groups in MMC as an example.

First, this paper presents the method which divides all sub-module cells into several groups. By using this grouping method, the number of cell voltage sampling per one sampling period can be reduced considerably. If the conventional sensing method without grouping method is used, the required number of cell voltage sensing is 6*N* at one sampling instant. In the proposed method, however, one of several groups is only sampled at a sampling instant. If the cells are divided into *m* sensing groups, the number of cell voltage data per one sampling point is reduced as 6*N*/*m*. For example, in the case of grouping 6 groups as shown like Fig. 2, the cell voltages in a group among 6 groups are sampled at one sampling instant. The corresponding sampling principle diagram can be shown in Fig. 3. Each sensing group comes around every 6 sampling points. The cell voltages of other 5 sensing groups, not sensed in that sampling instant, are estimated based on a scheme which will be mentioned in later sections of this paper.

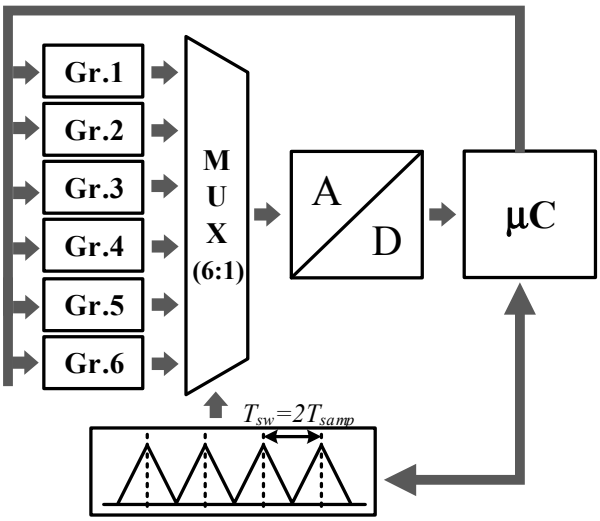

Figure 3. Sampling principle diagram for 6 sensing groups.

B. Estimation of Sub-module Cell Voltages

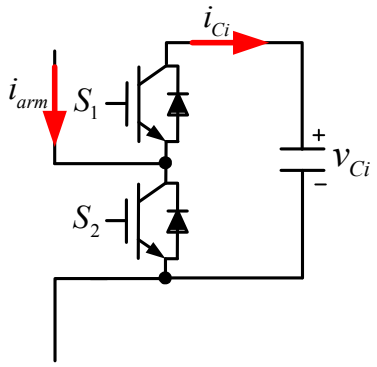

Figure 4. Circuit configuration of sub-module cell (half-bridge based cell).

TABLE I. SWITCHING DUTY AND CAPACITOR CURRENT

Duty	Gate signal $\{S_1, S_2\}$	i_{Ci}	$\hat{i}_{Ci}[k]$
$D_i = 1$	{1,0} : ON	$S_1 \times i_{arm}$	$D_i[k] \times i_{arm}[k]$
$D_i = 0$	{0,1} : OFF		
$0 < D_i < 1$	PWM		

Charging and discharging of cell capacitor is determined by capacitor current, i_{Ci} from switching states, { S_1 , S_2 }, and direction of arm currents, i_{arm} . This condition can be described by Fig. 4 and Table 1. As seen from the above figure and table, the capacitor current would be the value which is the arm current quantity multiplied by the duty ratio on the assumption that the arm current can be approximated as constant during one sampling period.

The sampled data from discrete time period can be obtained by arm current and cell voltage sensors. Once the value of the duty on each cell is identified in one sampling period, it is possible to obtain the value that is approximated by the real cell capacitor current as described by (1):

$$\hat{i}_{Ci}[k] = D_i^*[k] \times i_{arm}[k], \quad (1)$$

where the superscript "*" refers to the reference value and "^" means the estimated value. At each sampling points, the estimated cell capacitor voltage at next sampling point can be calculated by (2) simply, where $\hat{C}_i$ is the estimated value for the cell capacitance and is described in detail in the next paragraph.

$$\begin{aligned} v_{Ci}[k+1] &= v_{Ci}[k] + \frac{1}{\hat{C}_i} T_{samp} \times \hat{i}_{Ci}[k] \\ &= v_{Ci}[k] + \frac{1}{\hat{C}_i} T_{samp} \times D_i^*[k] \times i_{arm}[k]. \end{aligned} \quad (2)$$

The MMC system has 6N DC cell capacitors excluding the redundancy cells against the sub-module fault. These cell capacitors may have initial difference in the manufacturing stage and through aging. And, the cell voltage could be more accurately estimated, if the cell capacitance is estimated in on-line. The capacitance of sub-module cell capacitor can be estimated in real time as followings. The next sampled value of cell voltage in j-th group can be derived as (3) from the iteration of (2), where p is the number of group iterations and m is the number of groups:

$$v_{Ci}^*[(p+1)\cdot m + j] = v_{Ci}^*[p \cdot m + j] + \frac{T_{samp}}{\hat{C}_i} \sum_{k=p\cdot m+j}^{(p+1)\cdot m+j-1} \{D_i^*[k] \cdot i_{arm}[k]\} \quad (3)$$

$$\Delta v_{Ci}^* = v_{Ci}^*[(p+1)\cdot m + j] - v_{Ci}^*[p \cdot m + j]. \quad (4)$$

$$\Delta Q = T_{samp} \sum_{k=p\cdot m+j}^{(p+1)\cdot m+j-1} \{D_i^*[k] \cdot i_{arm}[k]\}. \quad (5)$$

$$\hat{C}_i = \frac{\Delta Q}{\Delta v_{Ci}^*}. \quad (6)$$

For simplifying (3), Δv_{Ci}^* and ΔQ can be defined by (4) and (5), respectively. And then, (6) can be derived from (3). The division in (6), however, may not be desirable because Δv_{Ci}^* may assume values very close to zero and the calculation process would be inaccurate. Furthermore, the effect of noise on the measurement may lead to an erroneous estimation of $\hat{C}_i$. And, an estimation algorithm using the adaptive observer for on-line parameter estimation is adopted in this paper. In Fig. 5 a control block diagram of the adaptive estimator with one unknown scalar parameter is shown [6]-[7]. The procedure for the estimation is given below. Using $\hat{C}_i$ as the estimate of C_i, the estimated or predicted value $\Delta\hat{Q}$ of the output ΔQ as $\Delta\hat{Q} = \hat{C}_i \Delta v_{Ci}^*$ is generated. The prediction or estimation error ε_1, which reflects the parameter uncertainty because $\hat{C}_i$ is

different from C_i, is formed as the difference between ΔQ and $\Delta\hat{Q}$ as shown like (7).

$$\varepsilon_1 = \Delta Q - \Delta\hat{Q} = \Delta Q - \hat{C}_i \Delta v_{Ci}^* . \quad (7)$$

The differential equation in (8) for generating $\hat{C}_i$ is developed by minimizing the simple cost criteria of ε_1 with respect to $\hat{C}_i$ [6].

$$\frac{d}{dt}C_1 = -\gamma \nabla J(C_i) = \gamma \nabla J(\Delta Q - \hat{C}_i \Delta v_{Ci}^*)\Delta v_{Ci}^* = \gamma \varepsilon_1 \Delta v_{Ci}^* , \quad (8)$$

where $\gamma > 0$ is a scaling constant or the adaptive gain.

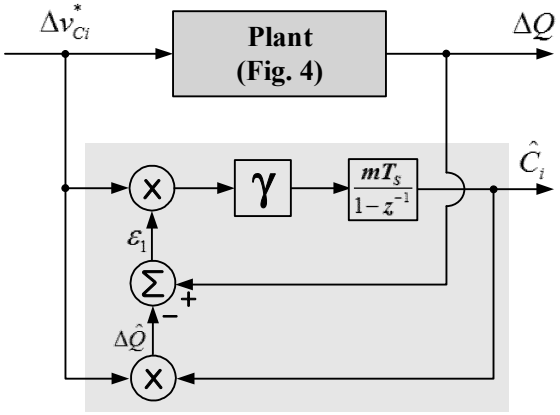

Figure 5. Adaptive observer in order to estimate the sub-module cell capacitance.

IV. Simulation Results

TABLE II. Circuit Parameters and Simulation Condition

Description	Abbreviation	Value
Line-to-line grid voltage	$V_{l-to-l,rms}$	200kVrms
Rated power	S_{mmc}	400MVA
DC-link voltage	V_{dc}	400kV
Rated grid current	I_{rated}	1155Arms
The number of cells in an arm	N_{total}	220 (including redundant cells)
Cell capacitor DC voltage	V_c	2.2kV
Cell capacitor	C_{cell}	4400μF

The proposed estimation scheme was validated by simulation studies in time-domain by PSIM software. The simulated MMC system is 400MVA, and the nominal number of cells in each arm, *N*, equals 200. The redundant sub-modules can also be prepared for failure of sub-modules in an arm. So, the number of the redundant cells is set as 20 (10%). The sampling frequency of processor is 10kHz and the capacitance of DC link of each cell is 4400μF. The parameters used in the simulation are summarized at Table 2.

In the simulation, the cell capacitors are divided into 12 groups. In other words, there are two groups per one arm. Therefore, the number of sampling data for cell capacitor voltages at every sampling instant can be decreased from 1320 to 110 which is one twelfth of the total number of sub-module cells.

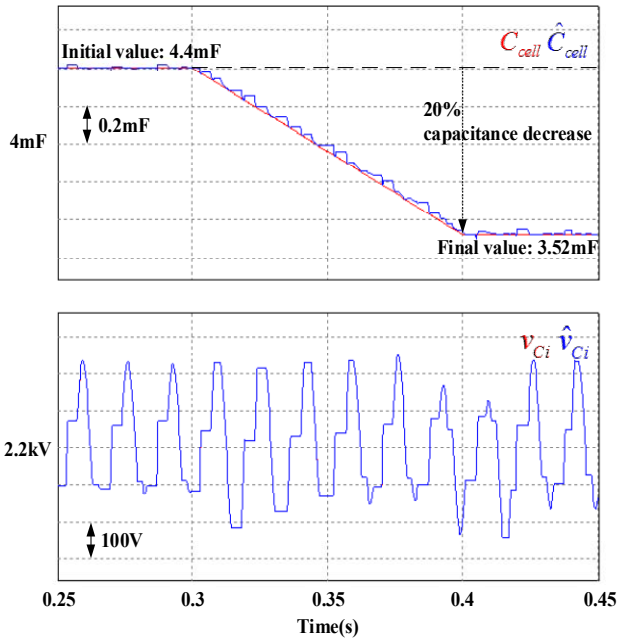

Figure 6. Simulation result: estimated capacitance and capacitor voltage.

In Fig. 6 the simulation results about estimation performance are shown. To verify the performance of the adaptive observer, the decreasing capacitance of a sub-module was simulated. At the time point, 0.3s, the cell capacitance of one sub-module starts to decrease from 4.4mF to 3.52mF (20% reduction). As shown in the figure, the output of adaptive observer, $\hat{C}_{cell}$, well tracked the emulated capacitance, C_{cell}. Due to the good performance of capacitance estimation, the cell capacitor voltage can be estimated almost exactly. And, the estimation with the proposed method was well performed in spite of 20% capacitance decrease within very short time, 0.1s.

Therefore, the capacitance of the cell capacitor can be monitored from the adaptive observer, and the proposed scheme can also reduce the cost of cell voltage sampling of a high level MMC.

V. EXPERIMENTAL RESULTS

(a) (b)

Figure 7. Experimental setup: (a) front of the MMC prototype, (b) back of the MMC prototype.

TABLE III. CIRCUIT PARAMETERS AND EXPERIMENTAL CONDITION

Description	Abbreviation	Value
Rated power	S_{mmc}	10kVA
DC-link voltage	V_{dc}	300V
The number of cells in an arm	N	6
Cell capacitor DC voltage	V_c	50V
Cell capacitor	C_{cell}	4400μF

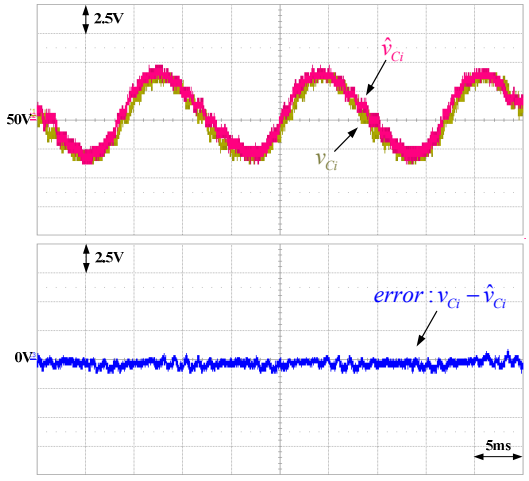

Figure 8. Experimental result: estimated capacitor voltage and estimation error.

A 10kVA prototype of 7-level MMC has been implemented in the laboratory. A photograph of prototype MMC is shown in Fig. 7, and the experimental conditions and parameters are presented in Table 3. The number of cells in each arm is 6. The sampling frequency is 5kHz and the cell capacitance is 4.4mF. In the experiment, the cell capacitors are divided into 6 groups. Therefore, the number of sampling data for cell capacitor voltages at one sampling instant was reduced from 36 to 6 which is a sixth of the total number of sub-module cells.

In Fig. 8, the experimental results with downscaled 10kVA MMC are shown. The overall control algorithm was executed with the estimated capacitor voltage values. And, the real value of cell capacitor voltage was measured for verifying the estimation performance. There is also little difference between the real and estimated capacitor voltage. The error between them is within 2%, which is under the allowable boundary.

VI. CONCLUSIONS

In this paper, an estimation strategy for reducing the cost of cell voltage sampling has been presented. To overcome the difficulties of handling the excessive sampling data, the many cells was grouped into several groups adequately. When the capacitor voltage value of a group is not updated at a certain sampling instant, an estimation scheme has been used to estimate the non-sampled cell voltage. The capacitance of the cell capacitor is also monitored from the adaptive observer for better cell voltage estimation. With the proposed method, the difference between the real and estimated values has been kept within allowable bound. The proposed scheme may contribute to reduce the cost of cell voltage sampling of a high level MMC for HVDC.

REFERENCES

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Industrial Electronics Magazine, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] Hagiwara, Makoto, Kazutoshi Nishimura, and Hirofumi Akagi. "A medium-voltage motor drive with a modular multilevel PWM inverter." Power Electronics, IEEE Transactions on 25.7 (2010): 1786-1799.

[4] Antonopoulos, Antonios, et al. "On interaction between internal converter dynamics and current control of high-performance high-power ac motor drives with modular multilevel converters." Energy Conversion Congress and Exposition (ECCE), 2010 IEEE. IEEE, 2010.

[5] Jung, Jae-Jung, Hak-Jun Lee, and Seung-Ki Sul. "Control of the Modular Multilevel Converter for variable-speed drives." Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on. IEEE, 2012.

[6] Ioannou, Petros A., and Jing Sun. "Robust adaptive control." Courier Dover Publications, 2012.

[7] Tao, Gang. Adaptive control design and analysis. Vol. 37. Wiley-IEEE Press, 2003.

[8] Kui Wang; Yongdong Li; Zedong Zheng; Lie Xu, "Voltage fluctuation suppression method of floating capacitors in a new modular multilevel

converter," Energy Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.2072,2078, 17-22 Sept. 2011.

[9] Jun Mei; Ke Shen; Bailu Xiao; Tolbert, L.M.; Jianyong Zheng, "A New Selective Loop Bias Mapping Phase Disposition PWM With Dynamic Voltage Balance Capability for Modular Multilevel Converter," Industrial Electronics, IEEE Transactions on , vol.61, no.2, pp.798,807, Feb. 2014.

[10] Bin Wu, "High-power Converters and AC Drives," Wiley-IEEE Press, 2006.

[11] Shi, Xiaojie; Wang, Zhiqiang; Tolbert, Leon M.; Wang, Fred, "A comparison of phase disposition and phase shift PWM strategies for modular multilevel converters," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE , vol., no., pp.4089,4096, 15-19 Sept. 2013.

[12] Hagiwara, M.; Akagi, H., "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," Power Electronics, IEEE Transactions on , vol.24, no.7, pp.1737,1746, July 2009