Layout of IGBT-based Current Source Converter for Low Stray Inductance

Sungho Jung, Hak-Jun Lee and Seung-Ki Sul
School of Electrical Engineering & Computer Science,
Seoul National University,
Seoul, 151-744, Korea
sungho@eepel.snu.ac.kr, hjlee@eepel.snu.ac.kr, sulsk@plaza.snu.ac.kr

***Abstract*—In this paper, a layout of Insulated Gate Bipolar Transistor(IGBT)-based Current Source Converter (CSC) to reduce stray inductance is proposed. Due to the rapid evolution of IGBT, it has become a competitive switching device in comparison with other high power switching devices even in MW power conversion system. The higher switching frequency of IGBT might reduce the size of other passive component of CSC significantly, and the demerits of CSC can be diminished remarkably, while the merits of CSC can be retained. However, since the switching speed of IGBT is high, the overshoot of the voltage across IGBT due to the stray inductance increases. And, the switching loss and voltage stress would be prohibitive. To decrease the stray inductance, a layout of power circuit exploiting magnetic coupling between bus bar connecting switching devices is devised in this paper. The stray inductances of two different layouts of IGBT-based CSC are compared to verify the effectiveness of the proposed strategy, experimentally.**

I. INTRODUCTION

The Current Source Converter topology has been used over multi mega-Watt power conversion due to its ruggedness to over current / short circuit and low dv/dt voltage over the load. In spite of those inherent virtues of CSC, in the last decade, it has been paid little attention for industry application because of the large passive components, limited switching frequency. In most application where the CSC-fed drive system has employed, gate turn-off thyristor(GTO) or integrated gate commutated thyristor(IGCT) has been used[1]-[2]. Recently, high-voltage IGBT(HV IGBT) has been evolved and it could be a switching device for CSC. Furthermore, IGBT might have a bidirectional voltage blocking capability, though none of high voltage IGBT has such a capability yet because the dominant market for HV IGBT is in voltage source inverter. If the IGBT is used as a switching device in CSC, the switching frequency of CSC can be increased over 1 kHz even in MW drive system. And, the cost and size of the passive components can be remarkably reduced. Additionally, HV IGBT has much higher di/dt capability than other switching devices such as GTO and IGCT. Hence, the external reactor is not required as a turn-on snubber. In addition, if the stray inductance of CSC is minimized in commutation loop, the turn-off snubber circuit, which is necessary to absorb the energy from stray inductance, would be saved even in higher switching frequency and MW drive[2]. In this paper, to reduce stray inductances, the magnetic coupled bus bar is proposed with considering commutation characteristic of CSC. And it is compared with normal bus bar layout where switching devises are located as close as possible to each other. Two different layouts are explained and total effective stray inductance of each case is calculated and compared. Also, the difference of the inductance is verified with the experimental prototype by measuring voltages across IGBT at switching.

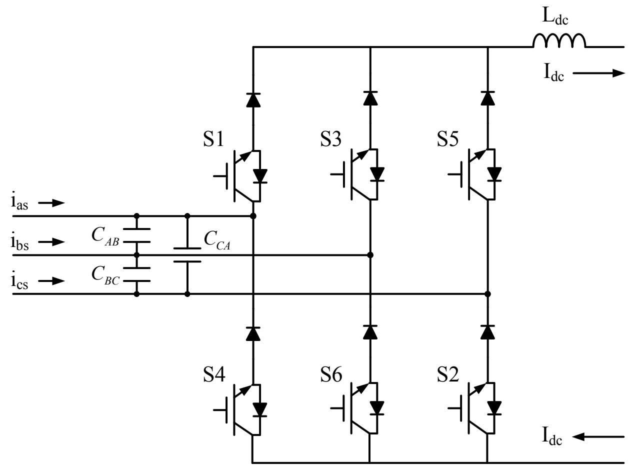


Fig. 1 IGBT-based CSC with reverse current blocking diode

II. COMMUTATION LOOP OF CSC

A. IGBT and Diode pair

In Fig.1, a circuit diagram of IGBT based CSC is shown together with input capacitor filter, where series connection of IGBT switch and diode is used because of no availability of the bidirectional voltage blocking IGBT[3]. Even, recently, the reverse blocking IGBT (RB-IGBT) module is used in Matrix Converter (MC) and advanced Neutral Point Clamped converter (Advanced NPC), the power rating is low and it is hard to control the turn on performance of RB-IGBT[4]. As IGBT switches and diode series connection are a reasonable in MW drive system, IGBT switch and diode series connected CSC is considered in this paper.

However, IGBT and diode should be connected in series and also three phases should be connected to other phase by wire or bus bar. These connections make unavoidable stray inductances in the commutation loop which enlarge a overshoot voltage when the switch is turned off.

978-1-4577-1216-6/12/$26.00 ©2012 IEEE

B. Space Vector in CSC

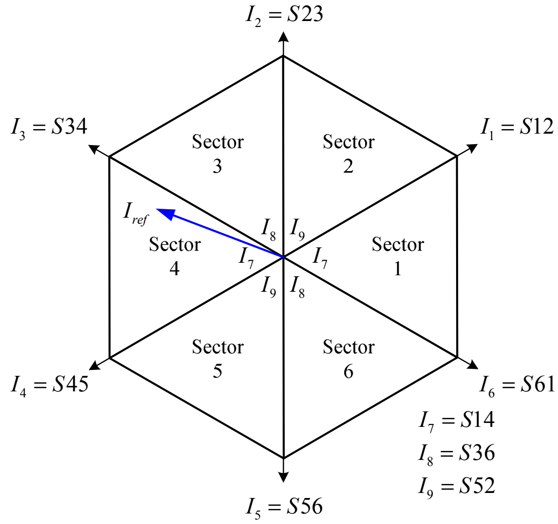


Fig. 2 Space Vector diagram of CSC

The space vector diagram in a current plane of CSC which has six sectors is shown in Fig 2. Six active vectors and three zero vectors can be applied according to the switching states. When an active vector is applied in CSC, the DC link current I_{dc} is pass through line to line filter capacitor which is connected with AC voltage source. So, the energy transfer and current variation would occur. When a zero vector is applied, the DC link current I_{dc} is bypassed from the filter capacitors, so there is no current variation and no energy transfer. When a current pass through the capacitor, it is divided according to the number of the capacitor in series. For example, when S1 and S6 are turned on, 2/3 of I_{dc} is passing through capacitor C_{AB} and 1/3 of I_{dc} is passing through capacitor C_{BC} and C_{CA} which are connected in series to AC terminal.

C. Classification of Commutation

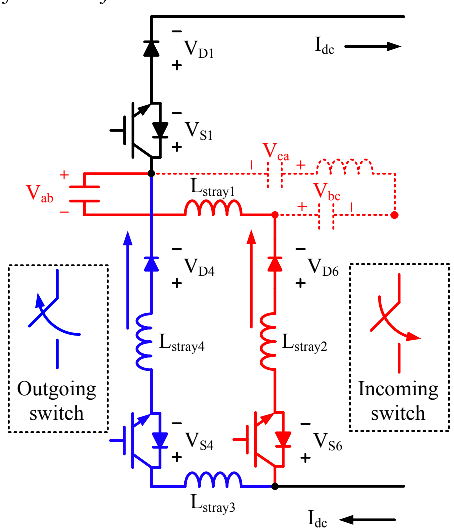


Fig. 3 Overall commutation loop of IGBT-based CSC
(Red: Increasing Current, Blue : Decreasing current)

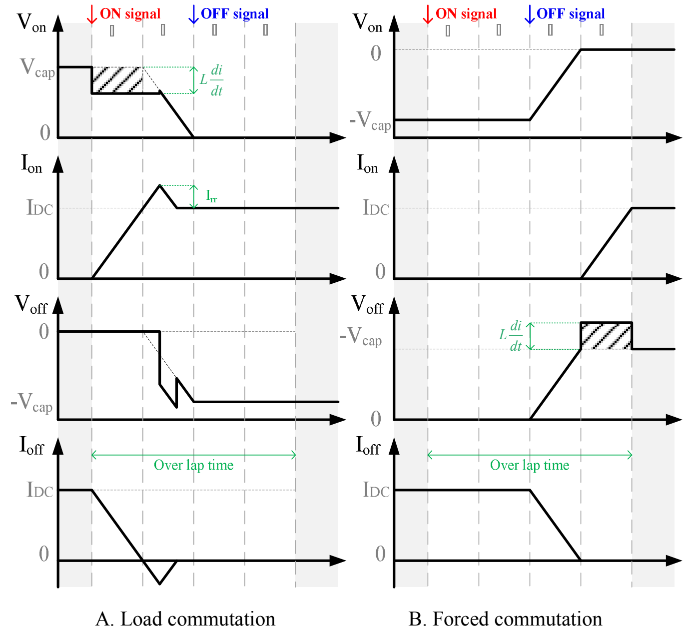


Fig. 4 Switch voltage and current wave form during commutation

A switch can be defined as an incoming switch, which is turning on, or an outgoing switch, which is turning off as shown in Fig 3. The voltage across the switch and current waveforms are shown in Fig 4. According to the filter capacitor voltage between the commutating switches, the commutating process can be classified as the load commutation or the forced commutation[5]. When the voltage across the incoming switch is positive, it is defined as the load commutation. In this case, the incoming switch current increases and the voltage across the incoming switch decreases right after the turn on signal. When the voltage across the incoming switch is negative, it is defined as the forced commutation. In this case, even if the ON signal is applied at the incoming switch, there are no currents and voltage change in both switches. After the OFF signal is applied at the outgoing switch, the voltage of the outgoing switch is increasing, and then, the current of the incoming switch increases.

Because of the stray inductance in commutation loop, the negative overvoltage across the outgoing switch pair(IGBT and diode) occurs due to the reverse recovery current of the diode at the load commutation. And, also, the positive overvoltage across the outgoing switch occurs due to the stray inductance of the commutation loop at the forced commutation. The magnitude of the overvoltage depends on the magnitude of the DC-link current, the switching transition time, and stray inductance. To prevent the overvoltage across a switch pair, slower turn-off strategy can be adopted by modifying gate driver circuit. However, it limits the switching frequency and augments switching loss. Thus, if possible, the minimization of the stray inductance is the right way to reduce switching loss and overvoltage across the switch pair simultaneously.

III. LAYOUT OF IGBT-BASED CSC STRUCTURE

A. Inductance calculation

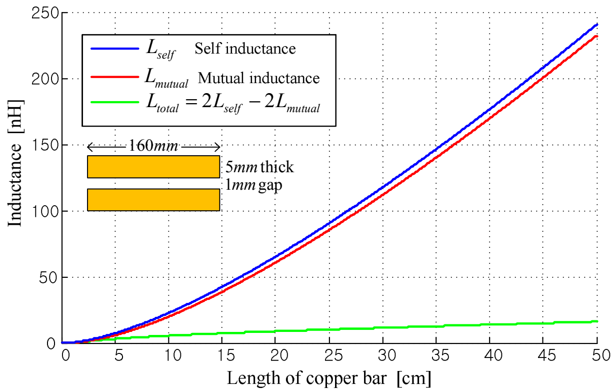


Fig. 5 The inductance value depend on a bus bar length

To calculate the effective stray inductance in the commutation loop, Fast Henry's Formula and Grove's Formula(1),(2) is used for the calculation of the self and mutual inductance calculations[5]~[8]. Also, Q3D Extractor, which is a simulation language based on FEM, is use to verify the calculated value by (1) and(2)[9].

$$L_{self} = \frac{\mu}{2\pi} l \left(\ln\left(\frac{2l}{b+c}\right) + \frac{1}{2} - \ln\left(\frac{b+c}{l}\right) \right) \qquad (1)$$

,where l : the length of busbar
b : the width of busbar
c : the height of busbar

$$L_{mutual} = \frac{\mu}{2\pi} l \left(\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}} \right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l} \right) \qquad (2)$$

,where l : lenth of bus bar
d : GMD of coupled bus bars

From Fig. 5, it can be seen that the inductance depends strongly on the length of bus bar, but the inductance are not a linear function of the length. To reduce the stray inductance in CSC, the length of the bus bar should be minimized. However, under some limitations of layout such as size of switching devices, terminal, and filter capacitor, the length cannot be reduced as desired. In this case, the total stray inductances can be reduced exploiting mutual inductances in commutation loop without reducing physical length of the bus bar itself.

B. Conventional structure

In Fig. 6, a conventional connection bus bar of CSC system using 1700V-1800A IGBT and diode is shown, where all components are connected like the circuit diagram. In the case of voltage source PWM power conversion, similar connection except the series diodes has been used. For the capacitor connection, Δ connection is the best option in the view point of stray inductance. The switching devices are laid as close as possible to each other to minimize the stray inductance.

In this bus bar layout, the smallest stray inductance of the commutation loop is around 60nH and the largest one is around 180nH. The values do not include the inductances inside of switching devices. The inner stray inductance of filter capacitors and switching devices is not considered. Based on the calculation, reducing the largest stray inductance in the loop is imminent, because the overvoltage due to the stray inductance would ask higher the voltage blocking capability of the switching device and results in the higher cost and worse characteristics[2].

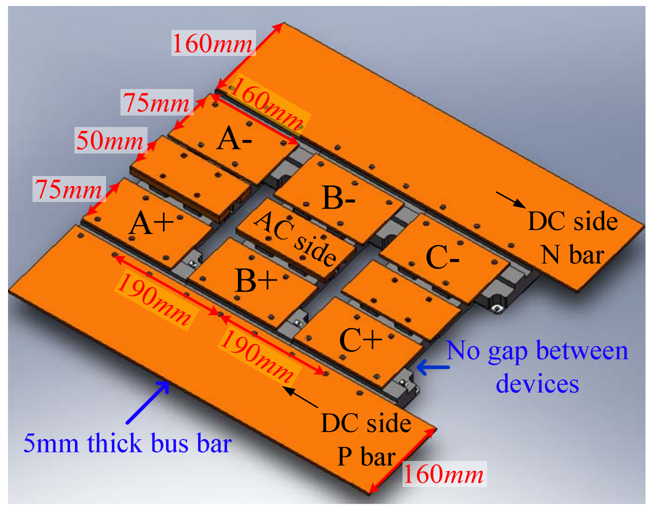
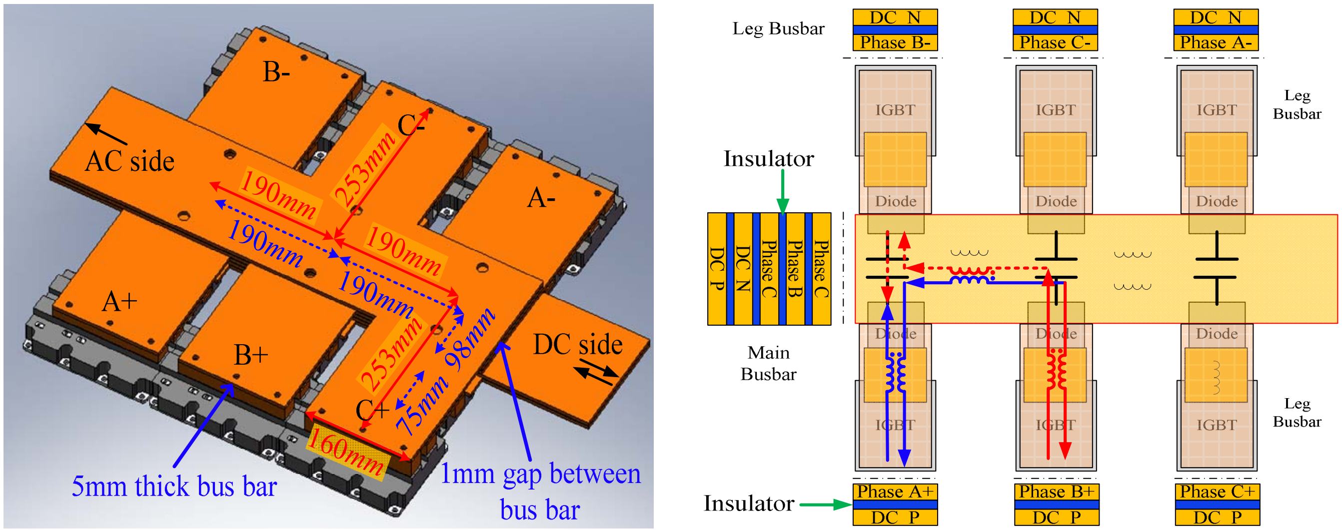


Fig. 6 Conventional bus bar connection of CSC system

C. Proposed magnetically coupled structure

In Voltage Source Converter (VSC), a parallel stacked bus structure, which has insulation between positive and negative bus plate of DC link, is commonly used to reduce the stray inductance in the commutation loop. Because the stacked bus bars are magnetically coupled to each other, the effective stray inductance is small even though the total length of the commutation loop is quite long [5]-[6]. To apply this concept to CSC, in this paper a magnetic coupled layout is proposed to reduce the stray inductances in Fig 7 after considering current path in the commutation loop. Firstly, a current return path is used to reduce the stray inductance between IGBT and Diode. Because the same current is passing through lower and upper bus bar with different direction, the mutual inductance reduces the effective inductances of the bus bar itself. Secondly, the twisted phase leg position such as A+B+C+ for upper switch and B-C-A- for lower switch, like Fig. 7, can maximize the magnetic coupling effect in the commutation. In here, the stacked bus bars in Fig.7, where the bus bars of DC P, DC N, Phase A, Phase B, and Phase C are stacked vertically, are used to reduce the stray inductance of three phases and DC link connectors. Through the twisted leg and the stacked bus bars,



(a) General view (b) Conceptual diagram

Fig. 7 Proposed bus bar connection of CSC system

one leg current rises, another one leg current falls simultaneously for any commutation process. Since the bus bars of rising and falling current are set in the same direction in this layout structure, the mutual inductance can reduce the effective stray inductance during the commutation process.

As an example of the commutation process with the proposed stacked bus bar, is assumed that the reference vectors, I_7, I_4, and I_3 in Fig2 are commutation in one sampling time. And, the current flow of this commutation process from I_7 to I_3 is shown in Fig. 8. A+ is outgoing switch and B+ is incoming switch. When the sign of Vab is minus, it is forced commutation. Both the rising current of phase B+ and the falling current of phase A+ have return path where the mutual inductance reduces the total inductance in the leg bus bar. The falling current of DC N and the rising current of phase B have same direction where also the mutual inductance reduces the total inductance in the main bus bar like Fig.7 (b). However, because the DC current pass through not only the C_{ba} but also the series connection of C_{bc} and C_{ca}, the rate of rising current of phase B and the rate of falling current of DC N is different. According to the capacitance of the current path, the total current is divided and flow like fig.8 (c). In Fig. 8 (b), the current flow diagram and the rate of the current variation at the commutation between S14 and S34 are shown. If all the capacitance of the filter capacitors is the same, in phase B 67% of the falling current in DC N would flow. The remaining 33% of the current passes through phase A and phase C bus bar. The applied voltage to the switch pair can be expressed like (2) by using KVL and dot-convention method.

$$V_{sw} = -V_{cap} + (L_{s\_in} - L_{m\_in})\frac{di_{inc}}{dt} - (L_{s\_out} - L_{m\_out})\frac{di_{dec}}{dt} + (L_{s\_main} - L_{m\_main})\frac{di_{inc}}{dt} \quad (2)$$

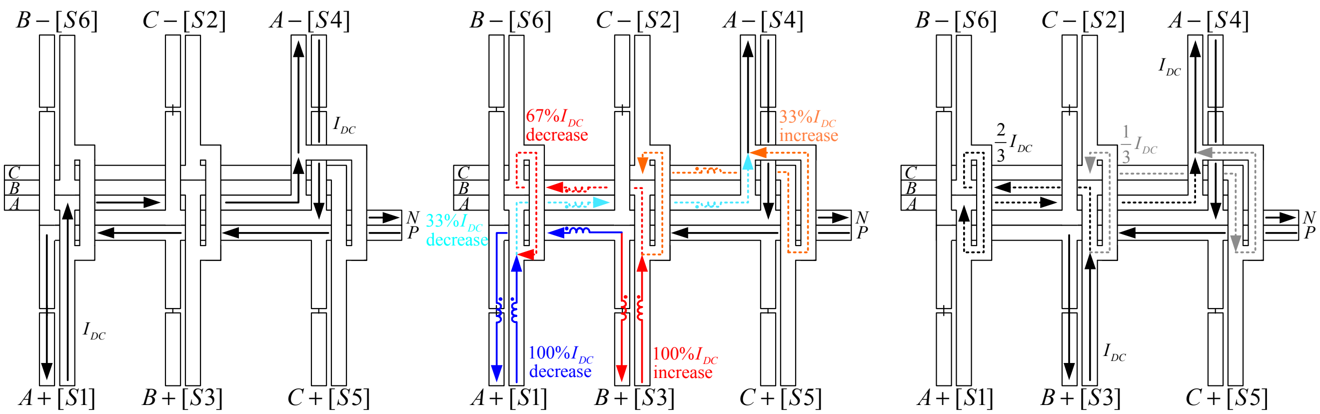
,where

V_{cap} : Filter capacitor voltage between commutation path
V_{sw} : Switch pair voltage of outgoing switch
L_{s_in} : Self inductance of incomming switch leg
L_{m_in} : Mutual inductance of incomming switch leg
L_{s_out} : Self inductance of outgoing switch leg
L_{m_out} : Mutual inductance of outgoing switch leg
L_{s_main} : Effective self inductance of main busbar
L_{m_main} : Effective mutual inductance of main busbar
di_{inc}/dt : Increasing current variation(red arrow)
di_{dec}/dt : Decreasing current variation(blue arrow)

Not only the case in Fig.8, but also every commutation case has similar mutual coupling effect with the proposed bus bar structure. The inductances are compared in Table1, through the calculation. With the proposed bus bar structure, the minimum inductance with shortest length of bus bar is 83nH as the total effective stray inductance in the path, the maximum one is 93nH. While the conventional structure, the minimum is 61nH but the maximum is 180nH. With the proposed layout, the maximum stray inductance, which is the deciding factor to blocking voltage of switching devices, is reduced by 54% compared to the conventional one. And, it is expected that the overvoltage stress due to the stray inductance can be reduced proportionally. Furthermore, with this strategy of bus bar layout, the space between power devices can be increased without the severe penalty of the stray inductance to accommodate high power devices or to increase cooling effects. Additionally, the filter capacitor can be easily assembled because of the twisted phase leg layout.

TABLE I. Comparison of stray Inductance from inductance calculation

	Inductance value [nH]		Variation [nH]
	Largest	***smallest***	
Conventional layout	180	61	119
Proposed layout	83	93	10



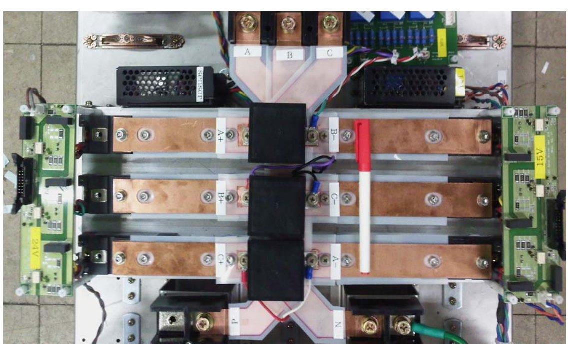
(a) Current flow at S14 (b) current variation ratio at commutation between S14 and S34 (c) Current flow at S34

Fig. 8 Current flow and current variation rate according to the switch state at sector 4

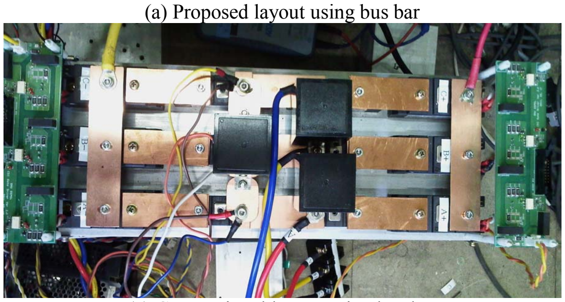
IV. Experiments

A. Experiment setup

In Fig. 9 (a), a photo of the scaled prototype of IGBT-based Current Source Inverter(CSI) and CSC with 1200V-75A IGBT(DM2G75SH12A) and Diode (DA2F75N12S) are shown. 1.5mm tick and 30mm wide magnetically coupled bus bar is used to connect each element. And whole CSC is assembled as shown in Fig. 7. Each device is spaced 10mm or 20mm apart for filter capacitor connection. For the insulation of the main bus bar stack, bus bars are laminated by poly urethane is spaced about 0.5mm each other, and insulation paper is inserted between them. For comparison, the conventional layout with the same size of bus bar and devices are also used and assembled as shown in Fig6. The photo of the conventional lay out is shown in Fig. 9(b).



(a) Proposed layout using bus bar



(a) Conventional layout using bus bar

Fig.9 Experiment setup for CSC

Switch voltage and DC link current during commutation are measured to calculate the stray inductance of a commutation loop[6]. A differential voltage probe, whose bandwidth is 100MHz, and a current probe, 2MHz, are used at the experiment. Also, to measure the current through the bus bar, a rogowski coil, 10MHz bandwidth, is used.

B. Current flow in the filter capacitor

In Fig. 10, the IGBT voltage of leg C+ and filter capacitor current of C_{AB} and C_{CA} are shown. Because a rogowski coil can't measure a DC component, the current values are biased as 0 at a zero vector S52. The DC link current is controlled around 35A. At state S12, the C_{CA} is parallel with series of C_{AB} and C_{BC}, so the 67% of DC link current is passing through C_{CA} and 33% of DC link current is passing through C_{AB}. At state S32, the C_{BC} is parallel with series of C_{CA} and C_{AB}, so the 33% of DC link current is passing through C_{CA} and C_{AB}. At the end of the S32, even S5 voltage is tuned on, no current is commutated because the turn on signal defines the current commutation in this case as explained in section Ⅱ C.

C. Overvoltage at Forced commutation

In Fig. 11 and Fig.12, the overshoot of the voltage and the DC link current are measured. The filter capacitor voltage also measured to compare with the overshoot voltage. The commutation between A+ and C+ has the largest stray inductance. Because the leg connecting bus bar length is longer than other cases and filter cap also far from those switches. The stray inductance from the experiment is 293nH. The commutation between A+ and B+, or B+ and C+ have the smallest stray inductance. Only two pieces of diode and switch connector and short length of leg connecting bus bar are existed in the commutation loop. The stray inductance is 213nH.

In magnetic coupled structure, because of magnetically coupled structure, the stray inductance difference between each case is not so large. The largest stray inductance is 194nH and the smallest on is 186nH. The experiment results and calculation results are compared in Table 2.

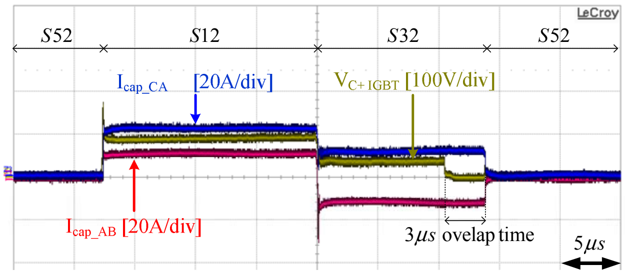
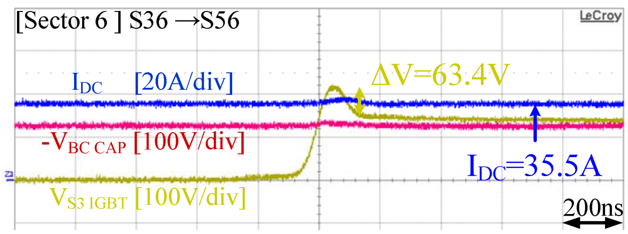
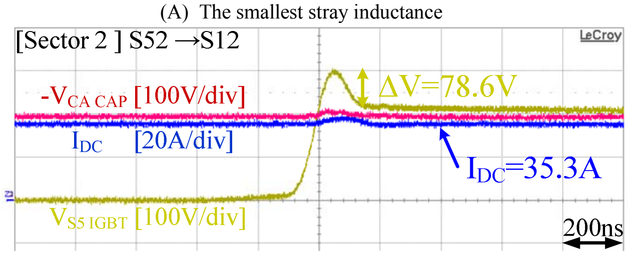


Fig.10 Capacitor currents(using a rogowski coil) and switch voltage at Sector2

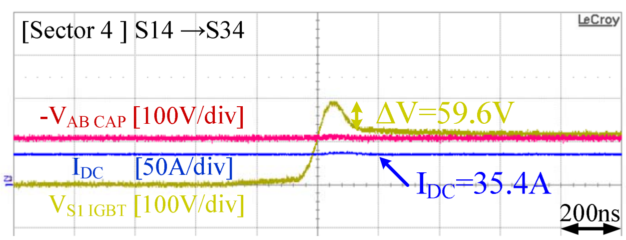


(A) The smallest stray inductance

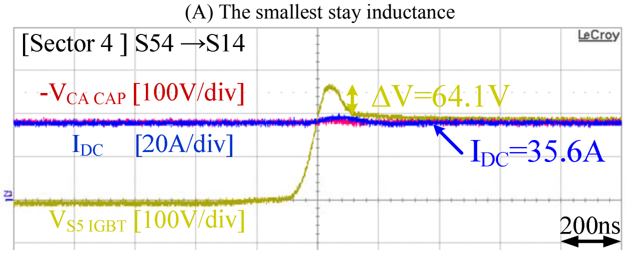


(B) The largest stray inductance case

Fig.11 The experiment result of the conventional layout case



(A) The smallest stay inductance



(B) The largest stray inductance

Fig.12 The experiment result of the proposed layout case

Because stray inductance is not a linear function of a bus bar length, the summation of each pieces of the stray inductance is different with the total stray inductance in a commutation loop. And also, the inner stray inductance of IGBT and Diode, whose nominal stray inductance is from 10 to 20nH in each, are not considered. The inner stray inductance of the filter capacitor is expected to be more than 10nH. For those reasons, the difference between calculation and experiment result is around 100nH.

From the estimated inductances, it can be seen that the largest stay inductance of coupled layout is around 66% of that of the conventional layout. And, the difference between the largest and the smallest one is 8nH in magnetic coupled bus bar. However, the difference in the conventional layout is 80nH. It means that the total stray inductance has less dependency on the distance between switching devices in the proposed layout, as expected.

TABLE II. Comparison of stray Inductance about prototype

		Stray inductance [nH]		
		$L_{largest}$	$L_{smallest}$	$L_{difference}$
Conventional Layout	Calculation	163	69	94
	Experiment	293	213	80
Magnetically Coupled Busbar	Calculation	90	75	15
	Experiment	194	186	8

V. CONCLUSION

In this paper, a magnetically coupled bus bar structure for IGBT-based CSC has been proposed. Because the IGBT has much higher di/dt capability than other switching devices, the magnetically coupled bus bar can be designed to save the turn-off snubber circuit, which is usually used for IGCT based CSC. To reduce the stray inductance, the current path during commutation is investigated to exploit the mutual coupling effects of bus bar. Also, the twisted phase leg is implemented to take advantage of the current variation in the commutation process. Hence, the maximum stray inductance can be reduced up to two third of the conventional layout case. From the experimental results, the magnetic coupling effect is verified. Because of the less total effective stray inductance and the reduced voltage overshoot, the operating voltage of CSC can be enhanced with the same blocking voltage IGBTs. Furthermore, because of the magnetically coupled bus structure, the spacing between devices of CSC would be flexible.

REFERENCES

[1] Y. W. Li, B. We, D. Xu, and N. Zargari, "Space vector squence investigation and synchronization methods for active front – end rectifiers in high-power current-source drives," *IEEE Trans. Power Electron.*, vol.55, no. 3, pp. 1022 – 1034, March 2008.

[2] H.F. Bilgin, and M. Ermis, "Design and implementation of a current-source converter for use in industry applications of D-STATCOM," IEEE Trans. Power Electron.,vol.25, no. 8, pp. 1943 – 1957, Aug. 2010.

[3] J. Espinoza, and G. Joos, "Current-source converter on-line pateern generator switching frequency minimization," *IEEE Trans. Ind. Electron.*, vol. 44, no. 2, pp. 198-206, April 1997.

[4] P. Grbovic, F. Gruson, N. Idir, and P. Moigne, " Turn-on performance of reverse blocking IGBT(RB IGBT) and optimization using advanced gate driver," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 970-980, April 2010.

[5] M. Abu-Khaizaran, and P.Palmer, “ Commutaion in high power IGBT based current source inverter,” PESC’07, pp. 2209-2215. 2007.
[6] G.L. Skibinski, and D.M. Divan, “Design methodology and modeling of low inductance planar bus structures,” EPE’ 93, pp. 98-105, Sep., 1993.
[7] M.C.vaponet, F. Profumo, R. De Doncker, and A. Tenconi, “Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits,” IEEE Trans. Power Electron., vol. 17, no. 2, pp. 225-231, March 2002.
[8] H. Kim, and C. C. Chen, “Be careful of self and mutual inductance formulae,” VLSI-EDA LAB, University Wisconsin, Madison, Technical Rep., 1999.
[9] Available : http://www.ansoft.com