Control Scheme for Source Voltage Sensorless PWM Converters under Source Voltage Unbalance

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Abstract

This paper presents a control scheme for three-phase PWM converters which have no ac-side voltage sensors. In spite of no source voltage sensors, the proposed method estimates exact grid angle and voltages, which are the essential parts for the power transfer between DC link of PWM converter and AC source. The method works not only in normal balanced AC source case but also in faulty unbalanced cases. The validity of proposed method has been evaluated by computer simulation and experimental result with 10kW PWM Voltage source converter.

1. Introduction

Recently, three-phase PWM voltage source converters have been widely used in industrial applications where bidirectional power control capability with reduced harmonic current is required. Detailed description of the PWM converter has been introduced in [1]–[3]. In [2], [3], the current regulators have been implemented in the synchronously rotating reference frame to reduce the steady state current regulation error. However, if there is a source voltage unbalance in a three-phase system, it gives rise to voltage ripples in the dc-link, increases the reactive power, and makes the performance of current regulators be degraded [4]. In [4], a method controlling positive and negative sequence of the voltage independently has been proposed to improve dynamic performance of current controller under source voltage unbalance. And a current reference generation algorithm has been introduced to reduce the voltage ripple in dc-link [5], [6].

However, in all the methods described in [1]–[6], a considerable number of feedback signals are required. To reduce the cost of a PWM converter, different control methods so called sensorless control have been proposed [7]–[14]. In [7]–[11], a source voltage sensorless control method estimating source voltages to save the source voltage sensors have been investigated. And to reduce the number of current sensors, phase current reconstruction technique has also been introduced [12]–[14]. Because the phase current reconstructions is not related to control scheme but modulation strategy, the phase current reconstruction can be applied to most of source voltage sensorless control schemes and it is out of this discussion. Though a lot of paper has been published in the topic of voltage sensorless control of PWM converter [7]–[11], as far as authors' knowledge, source voltage unbalances have not been much considered. In [10], an estimation of positive and negative source voltages has been proposed but its current control performance is limited and there was the current distortion in the case of a sudden source voltage change.

In this paper, a positive and negative sequence current controller for voltage sensorless PWM voltage source converter is adopted to improve dynamic performance under source voltage unbalances. And a source voltage observer based on mathematical model of overall system is designed to improve the disturbance rejection performance against a sudden change of the source voltage. Simulation and experimental results are shown in order to verify the feasibility of the proposed control scheme.

2. Mathematical Model under Source Voltage Unbalance

A structure of the source voltage sensorless PWM converter which is connected to the grid by an interface inductor is shown in Fig. 1. The output voltage of the PWM converter in stationary reference frame can be expressed as:

$$\boldsymbol{v}_{dq}^{s} = R_s \boldsymbol{i}_{dq}^{s} + L_s \tfrac{d}{dt} \boldsymbol{i}_{dq}^{s} + \boldsymbol{e}_{dq}^{s} \tag{1}$$

where $\boldsymbol{v}_{dq}^{s} \equiv \frac{2}{3}\left(v_a + e^{j\frac{2\pi}{3}} v_b + e^{-j\frac{2\pi}{3}} v_c\right)$, $\boldsymbol{i}_{dq}^{s} \equiv \frac{2}{3}\left(i_a + e^{j\frac{2\pi}{3}} i_b + e^{-j\frac{2\pi}{3}} i_c\right)$, $\boldsymbol{e}_{dq}^{s} \equiv \frac{2}{3}\left(e_a + e^{j\frac{2\pi}{3}} e_b + e^{-j\frac{2\pi}{3}} e_c\right)$ represent converter output voltage, line current, and source voltage, respectively. And R_s and L_s are resistance and inductance of the interface inductor.

For a three wire system, unbalanced three-phase source voltages can be decomposed into two balanced sets of positive and negative sequence components [4]:

$$\boldsymbol{e}_{dq}^{s} = \boldsymbol{e}_{dq.p}^{+} e^{j\omega_e t} + \boldsymbol{e}_{dq.n}^{-} e^{-j\omega_e t} \tag{2}$$

where $\boldsymbol{e}_{dq.p}^{+} = e_{d.p}^{+} + j e_{q.p}^{+}$ is a positive sequence component of the source voltage, $\boldsymbol{e}_{dq.n}^{-} = e_{d.n}^{-} + j e_{q.n}^{-}$ is a negative sequence component. The superscript '+' and '−' denote that corresponding variable is represented in the positive and negative sequence synchronous reference frame, respectively. ω_e is the angular frequency of the grid.

In a similar way, positive and negative sequences of the three-phase converter output currents can be decomposed like (3).

$$\boldsymbol{i}_{dq}^{s} = \boldsymbol{i}_{dq.p}^{+} e^{j\omega_e t} + \boldsymbol{i}_{dq.n}^{-} e^{-j\omega_e t} \tag{3}$$

where $\boldsymbol{i}_{dq.p}^{+} = i_{d.p}^{+} + j i_{q.p}^{+}$ and $\boldsymbol{i}_{dq.n}^{-} = i_{d.n}^{-} + j i_{q.n}^{-}$ are positive and negative sequence current components.

Applying (2) and (3) to (1) and equating the terms of positive sequence and the terms of negative sequence separately, the voltage equation can be decomposed into two subsystems as follow:

$$\boldsymbol{v}_{dq}^{s} = \boldsymbol{v}_{dq.p}^{+} e^{j\omega_e t} + \boldsymbol{v}_{dq.n}^{-} e^{-j\omega_e t} \tag{4}$$

where

$$\begin{aligned} \boldsymbol{v}_{dq.p}^{+} &= R_s \boldsymbol{i}_{dq.p}^{+} + L_s \tfrac{d}{dt} \boldsymbol{i}_{dq.p}^{+} + j\omega_e L_s \boldsymbol{i}_{dq.p}^{+} + \boldsymbol{e}_{dq.p}^{+} \\ \boldsymbol{v}_{dq.n}^{-} &= R_s \boldsymbol{i}_{dq.n}^{-} + L_s \tfrac{d}{dt} \boldsymbol{i}_{dq.n}^{-} - j\omega_e L_s \boldsymbol{i}_{dq.n}^{-} + \boldsymbol{e}_{dq.n}^{-} \end{aligned} \tag{5}$$

Because all of positive and negative sequence variables are expressed at positive and negative synchronously rotating reference frame, respectively, they have dc values in the steady state condition.

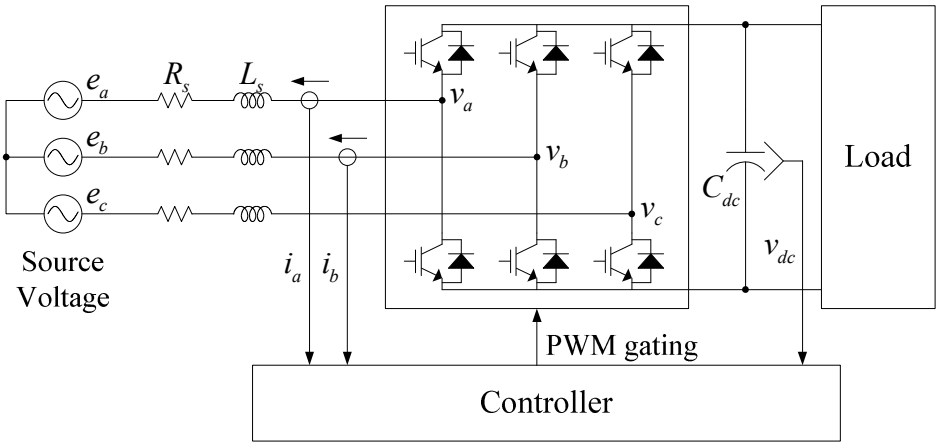


Fig. 1. Structure of a source voltage sensorless PWM voltage source converter

3. Proposed Control Scheme

The proposed control scheme consists of a current controller, a source voltage observer and a grid angle observer, and the overall system is shown in Fig. 2 as a control block diagram.

3.1. Current Controller

The basic structure of the proposed current controller is based on positive and negative synchronous reference frame PI controllers and its output voltage can be written as (6).

$$\begin{aligned} \boldsymbol{v}_{dq.p}^{+*} &= \left(\tfrac{1}{2}K_p\boldsymbol{i}_{dq.err}^{+} + K_i\int \boldsymbol{i}_{dq.err}^{+}dt\right) + j\hat{\omega}_e L_s \boldsymbol{i}_{dq.p}^{+} + \hat{\boldsymbol{e}}_{dq.p}^{+} \\ \boldsymbol{v}_{dq.n}^{-*} &= \left(\tfrac{1}{2}K_p\boldsymbol{i}_{dq.err}^{-} + K_i\int \boldsymbol{i}_{dq.err}^{-}dt\right) - j\hat{\omega}_e L_s \boldsymbol{i}_{dq.n}^{-} + \hat{\boldsymbol{e}}_{dq.n}^{-} \end{aligned} \tag{6}$$

where K_p and K_i stand for the proportional and integral gains, and the '$*$' stands for that the corresponding variable is a reference. And the '^', for the estimated value. The voltage output consists of three terms; the first one is from PI feedback control, the second term is for the decoupling of the d-q cross coupling effect, and the third one is the term for feed forwarding of the source voltage. Although the source voltage can be compensated by PI feedback controller, to achieve better transient performance a source voltage observer has been designed which is described in the next chapter. Under unbalanced condition, the current feedback can contain negative sequence component and can be represented as:

$$\boldsymbol{i}_{dq}^{+} = \boldsymbol{i}_{dq.p}^{+} + \boldsymbol{i}_{dq.n}^{-}e^{-2j\hat{\omega}_e t} \tag{7}$$

In the conventional way, the positive sequence controller is designed to eliminate the positive sequence current error against the positive sequence current reference. Thus, to achieve better control performance, the positive sequence current has to be properly extracted from the line current feedback. To do this, a notch filter can be applied to (7) [6], but in that case the dynamic performance of current control would be degraded. In this paper, to keep the control performance, the current errors are calculated by:

$$\begin{aligned} \boldsymbol{i}_{dq.err}^{+} &= \boldsymbol{i}_{dq}^{s*}e^{-j\hat{\omega}_e t} - \boldsymbol{i}_{dq}^{+} \\ \boldsymbol{i}_{dq.err}^{-} &= \boldsymbol{i}_{dq}^{s*}e^{j\hat{\omega}_e t} - \boldsymbol{i}_{dq}^{-} \end{aligned} \tag{8}$$

where $\boldsymbol{i}_{dq}^{s*} = \boldsymbol{i}_{dq.p}^{+*}e^{j\hat{\omega}_e t} + \boldsymbol{i}_{dq.n}^{-*}e^{-j\hat{\omega}_e t}$.

According to this equation, the current error for positive sequence controller is total current error expressed in positive sequence synchronous frame. And thus two current controllers cannot be strictly separated, because the positive sequence controller also reacts to the negative sequence error. And the negative sequence controller also reacts to the positive sequence error. However, if the twice of synchronous frequency is inside of the current control bandwidth, this coupling effect can be neglected.

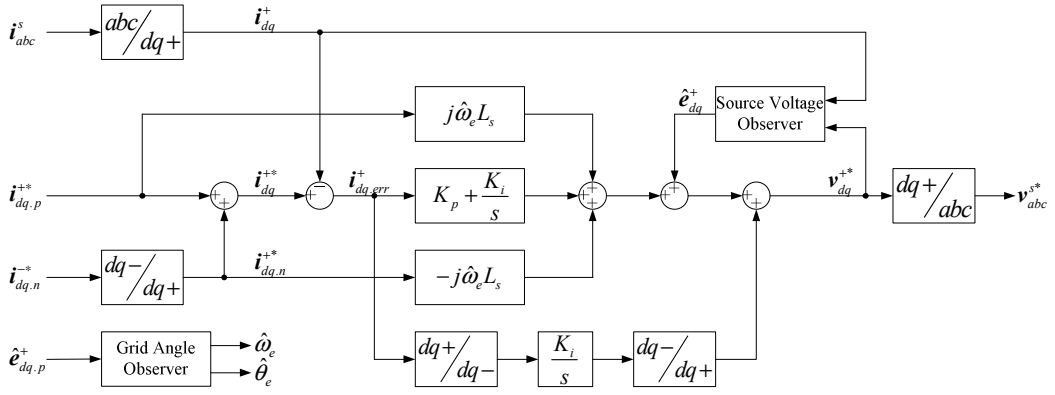


Fig. 2: Block diagram of the proposed control scheme

Assuming the source voltage and cross coupling terms are well compensated by feed forwarding terms, the closed loop dynamics of the controller is determined solely by the PI controllers. By the relationship between frame transformation and integrator which is well explained in [15], the output voltage transfer function can be described as (9).

$$\boldsymbol{V}_{dq}^{+*}(s)=\left(K_p+\frac{K_i}{s}+\frac{sK_i}{s^2+\left(2\hat{\omega}_e\right)^2}\right)\left(\boldsymbol{I}_{dq}^{+*}(s)-\boldsymbol{I}_{dq}^{+}(s)\right) \tag{9}$$

And the closed loop transfer function becomes as (10).

$$\boldsymbol{I}_{dq}^{+}(s)=\frac{K_p+\frac{K_i}{s}+\frac{sK_i}{s^2+\left(2\hat{\omega}_e\right)^2}}{R_s+sL_s+K_p+\frac{K_i}{s}+\frac{sK_i}{s^2+\left(2\hat{\omega}_e\right)^2}}\boldsymbol{I}_{dq}^{+*}(s). \tag{10}$$

Fig. 3 shows Bode plot of (10) when $K_p=\omega_{cc}L_s$ and $K_i=\omega_{cc}R_s$ where ω_{cc} is a cut-off frequency of the closed loop controller assuming that the transfer function is 1st order low pass filter. When the cut-off frequency of the current controller is 500Hz, the difference between with and without negative sequence controllers is negligible. On the other hand, when the cut-off frequency of the current controller is set as 100Hz, the overshoot near the twice of the grid frequency increases conspicuously. Thus, to achieve the ideal 1st order low pass filter dynamics in the positive synchronous reference frame, the cut-off frequency has to be increased as much as possible. Moreover, because the positive and negative sequences are symmetric as shown in (6), the same performance can be expected in the case of the negative sequence components.

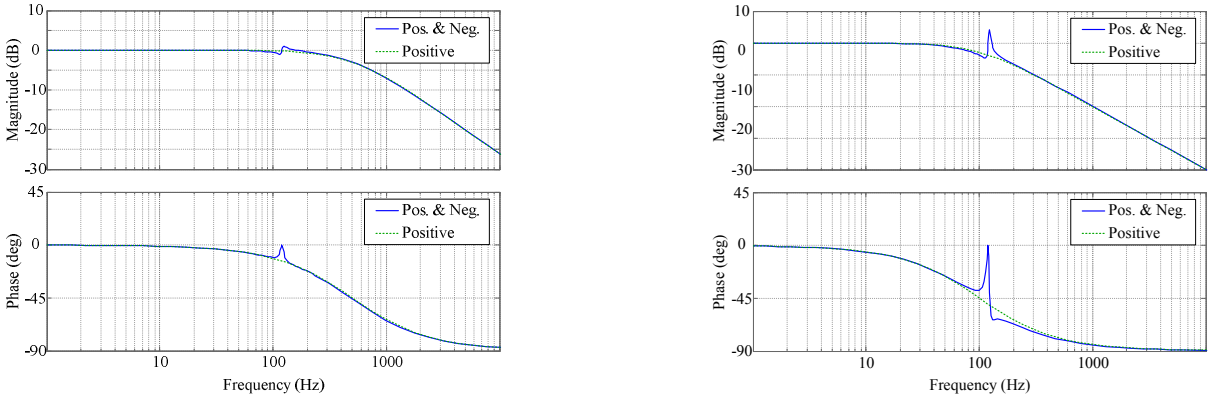


Fig. 3: Bode plot of the closed loop current controller; $\omega_{cc}=500Hz$ (left) and $\omega_{cc}=100Hz$ (right)

3.2. Source Voltage Observer

In the current control of PWM converter, the source voltages can be regarded as disturbances. For the disturbance rejection, a source voltage observer is designed as shown in Fig. 4. In order to construct a closed-loop observer, disturbance voltages are augmented as a state variable to be estimated by the observer as described in [16].

$$\frac{d}{dt}\hat{x}=\begin{bmatrix}-\frac{r_s}{L_s} & \omega_r & -\frac{1}{L_s} & 0\\ -\omega_r & -\frac{r_s}{L_s} & 0 & -\frac{1}{L_s}\\ 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\end{bmatrix}\hat{x}+\begin{bmatrix}\frac{1}{L_s} & 0\\ 0 & \frac{1}{L_s}\\ 0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}v_{ds}^r\\ v_{qs}^r\end{bmatrix}+\begin{bmatrix}L_1\\ L_2\end{bmatrix}\left(y-\hat{y}\right) \tag{11}$$

where $x = \begin{bmatrix} i_d^+ & i_q^+ & e_d^+ & e_q^+ \end{bmatrix}^T$ and $y = \begin{bmatrix} i_d^+ & i_q^+ \end{bmatrix}^T$. And to place all system poles identically at $-\alpha$ of Laplace domain, the feedback gain vector can be derived as (12).

$$\begin{bmatrix} L_1 \\ L_2 \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} + 2\alpha & \omega_r \\ -\omega_r & -\frac{R_s}{L_s} + 2\alpha \\ -\alpha^2 L_s & 0 \\ 0 & -\alpha^2 L_s \end{bmatrix} \tag{12}$$

Because the estimated voltages contain not only positive sequence components but also negative components, negative sequence integrators are added inside of the voltage observer in the same manner of the current controller, which is also shown in Fig.4.

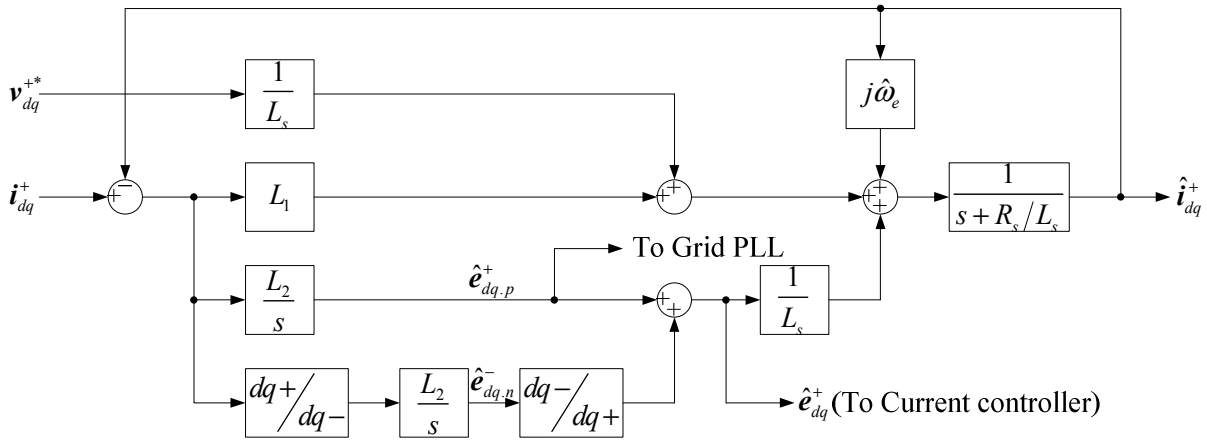


Fig. 4: Block diagram of the source voltage observer.

3.3. Grid Synchronization

Because the angular frequency of source voltage is usually quite constant, the grid angle which makes synchronous d-axis voltage be zero is estimated by a phase locked loop. If there is a source voltage unbalance, input of the phase locked loop is fluctuated and this makes the estimated grid angle fluctuate [17]. And because this fluctuation of the angle causes ac-side harmonic current with the current regulation loop of PWM converter, a positive sequence voltage angle observer has been devised. The relation between real grid angle and estimated one can be written as (13).

$$\begin{bmatrix} \hat{e}_{d.p}^+ \\ \hat{e}_{q.p}^+ \end{bmatrix} = \begin{bmatrix} -\hat{e}_{q.p}^+ \sin\left(\theta_e - \hat{\theta}_e\right) \\ \hat{e}_{q.p}^+ \cos\left(\theta_e - \hat{\theta}_e\right) \end{bmatrix} \tag{13}$$

Assuming the angle error is small, that is, $\theta_e - \hat{\theta}_e \ll 1$, the positive d-axis voltage can be approximated by

$$\hat{e}_{d.p}^+ \approx -\hat{e}_{q.p}^+ \left(\theta_e - \hat{\theta}_e\right). \tag{14}$$

As shown in Fig. 5, precise grid angle of the positive sequence component can be obtained by (15).

$$\hat{\omega}_{e.pi} = -\left(K_{p.pll} + \frac{K_{i.pll}}{s} \right) \hat{e}^{+}_{d.p} + \omega_{ff}$$
$$\hat{\theta}_e = \frac{1}{s} \hat{\omega}_{e.pi} \tag{15}$$

where $K_{p.pll} = \sqrt{2}\omega_{pll} / E_{nominal}$ and $K_{i.pll} = \omega_{pll}{}^2 / E_{nominal}$ are proportional and integral gain of PLL, respectively. ω_{pll} is the cut-off frequency of the PLL and $E_{nominal}$ is the nominal magnitude of the grid voltage. Usually, PI type regulator is applied to PLL to satisfy the transient performance. Because the estimated grid frequency changes very slowly, the sum of the integrator output and feed forwarding frequency is used as the estimated gird frequency.

When the converter operation starts, the nominal voltage of the grid is already known, however, the initial grid angle error may result in poor source voltage feed forward. This may invoke a high in-rush current and undesirable boost of the dc-link voltage. Thus, the initial grid angle has to be estimated to prevent over-current and dc-link over voltage trip. In order to obtain the initial value of the grid angle, the output voltage references of the PWM converter are adjusted to zero from the beginning of the switching and it lasts for a short period not to trip the over-current protection. During the zero voltage period of the PWM converter, the voltage equation can be simplified as:

$$\boldsymbol{e}^{s}_{dq} \approx -L_s \frac{d}{dt} \boldsymbol{i}^{s}_{dq} + \boldsymbol{v}^{s}_{dq}$$
$$\Rightarrow \hat{\boldsymbol{e}}^{s}_{dq} \approx -L_s \frac{\Delta \boldsymbol{i}^{s}_{dq}}{\Delta t} \tag{16}$$

where Δt is the PWM zero voltage period. From this equation, the initial source voltage can be estimated. And the initial angle can be obtained by (17) from the measurement of the ac line currents during this period [11].

$$\hat{\theta}_{e.initial} \approx \arctan\left(-\frac{\Delta i^{s}_{d}}{\Delta i^{s}_{q}} \right) \tag{17}$$

And then, the initial grid angle and source voltages are updated to the source voltage observer. In this way, the grid angle observer can reduce the initial transient time.

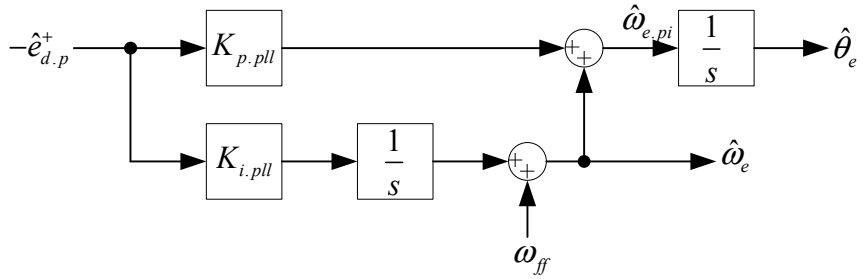


Fig. 5: Block diagram of the grid angle observer.

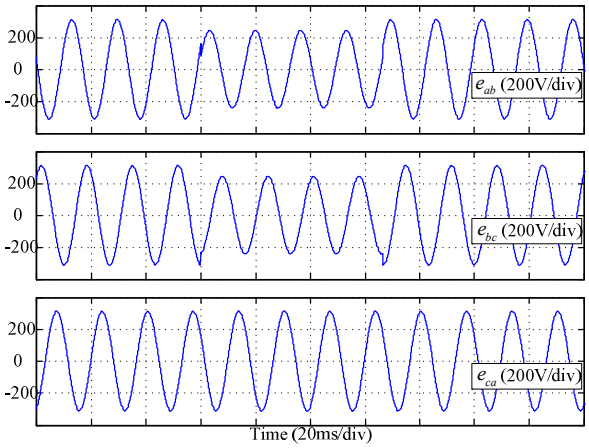
4. Simulation Results

To evaluate the feasibility of the proposed control scheme, a computer simulation has been performed by MATLAB. All of controllers are implanted in discrete time domain. And the poles of the current controllers and voltage observers are set as 500Hz and 200Hz, respectively. Value of the interface inductor L_s and R_s are set as 1.5mH and 100mΩ. To figure out the control performance, B phase voltage is reduced to 50% of the nominal value near the peak of the B phase voltage.

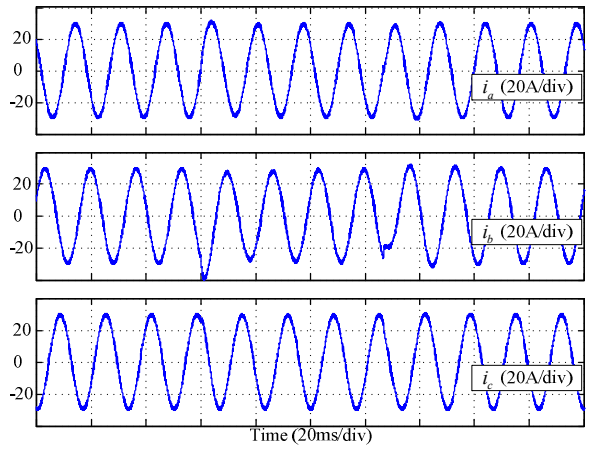
Fig. 6 shows the performance of feedback control during the voltage sag. Fig. 6(a) and (b) depict line-to-line voltage of the grid whose nominal values is 220Vrms/60Hz, and regulated three-phase line currents whose reference is 30A. Fig. 6(c) shows *d-q* current in synchronously rotating reference frame of (b). Because of the step voltage change, the currents are distorted but return back within 5ms,

while, the residual 120Hz components last for 20ms. Fig. 6 (d) and (e) show estimated positive and negative source voltages. In spite of sudden source voltage unbalance, the voltage observer estimates accurate source voltage within one cycle of source voltage. To compare with the real values, the positive and negative d-q voltages by the method introduced in [17] are drawn together. Fig. 6 (f) shows the trace of the estimated grid angle of which error is kept small enough during the voltage sag.

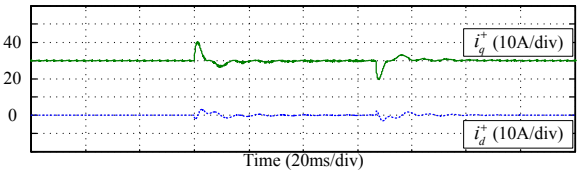
Fig. 7 shows current control performance against the reference changes. The left figure shows the current reference and feedback expressed in positive synchronous reference frame. The right top and bottom figures depict current errors in positive and negative synchronous reference frame, respectively. The positive q-axis current reference changes from -10A to -30A at the time point of 20ms. And the negative q-axis current reference changes from 0A to -10A at the time point of 70ms. Considering the bandwidth of the current control loop is set as 500Hz, the rise time of both cases is less than 1ms. From the results, and the bandwidth of the controller is near the set value.



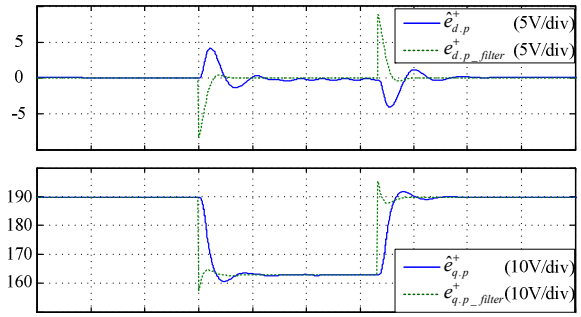
(a) Line-to-line voltages



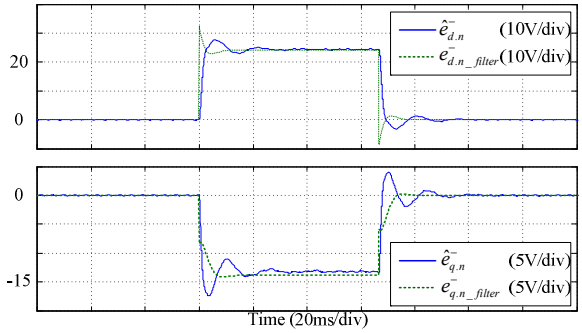
(b) Line currents



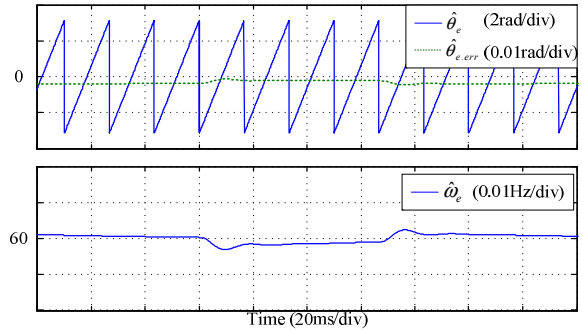
(c) Synchronous *d-q* feedback current



(d) Estimated positive *d-q* source voltage

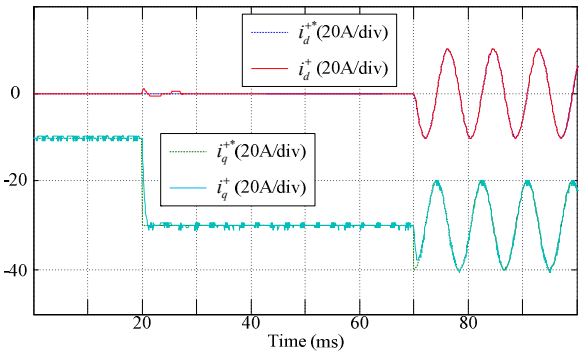


(e) Estimated negative *d-q* source voltage

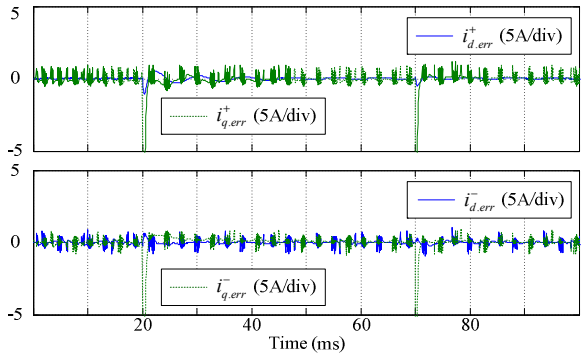


(f) Estimated grid angle and frequency

Fig. 6: Simulation result of current control and voltage estimation during a voltage sag.



(a) Current reference and feedback



(b) Current errors

Fig. 7: Simulation result of current control performance for step reference changes.

5. Experimental Results

To evaluate the validity of the proposed control scheme, an experiment has been performed. Fig. 8 shows the whole system configuration which consists of two PWM converters; one is target sensorless converter and the other is a load. Because they are connected to two different grids, the output power of one converter transferred to the other converter. The target PWM converter has been connected to an isolated AC power supply (MX 30, California Instrument Co.) to simulate source voltage sag. And the parameters of the experiment system are shown in Table I. The gains of current controller and source voltage observer have been set as the same with the case of the computer simulation.

Fig. 9 shows the experimental result of current control and voltage estimation during the voltage sag. It is assumed that the voltage sag is caused by the single line fault (Fault Type C [18]). And thus B phase voltage changed to half of the nominal value for four cycles. Because the experimental setup is a three-wire system, it undergoes only the line-to-line unbalance. From top to bottom in Fig. 9(a), the first one shows three-phase voltage of AC power supply and second one shows a line-to-line voltage e_{ab}. And phase A and B currents are shown in last two figures. Fig. 9(b) depicts feedback currents in synchronous reference frame. Distortion caused by sudden voltage unbalance is well compensated within a short period, 5ms. The estimated positive and negative source voltage is represented in Fig. 9(c). The source voltage observer estimates accurate source voltage in the average point of view but it contains some harmonic components which are generated by non-linearity of the PWM converter such as dead time and current sampling noise. Because of PWM output delay, these harmonic components may cause current harmonics. To avoid this, a low pass filter can be added to the output of the voltage observer. Fig. 9(d) describes the performance of grid angle synchronization. In spite of large unbalance voltage, there is no 120Hz harmonics in the estimated grid angle and frequency. The constant rate of change in the grid frequency is due to the AC power supply frequency variation during unbalance voltage generation.

Fig. 10 shows experimental result of the step response against current reference changes. The left one, (a), is the trace of the positive q-axis current reference changing from -10 to -30A. The right one, (b), is the trace of the negative q-axis current reference changing from 0 to -10A. As shown in figure, the rise times of both cases are less than 0.8ms. It means that the bandwidth of the controller is about 500Hz, which well matches to the set value, 500Hz.

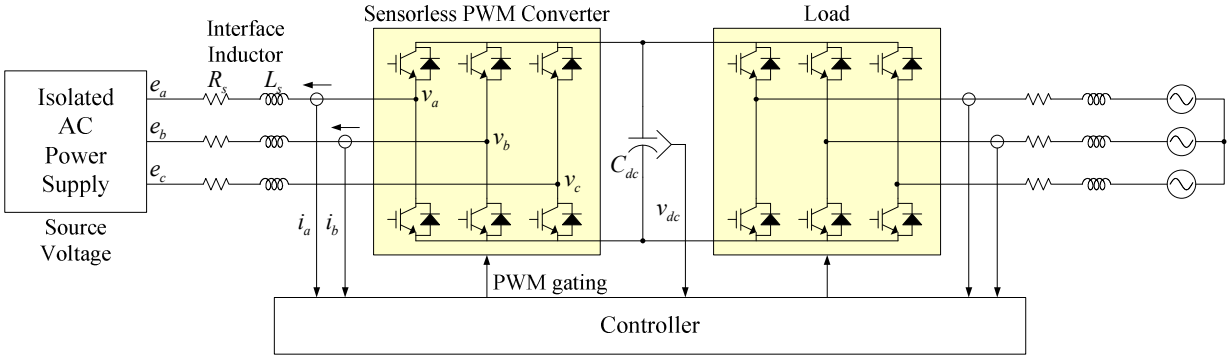
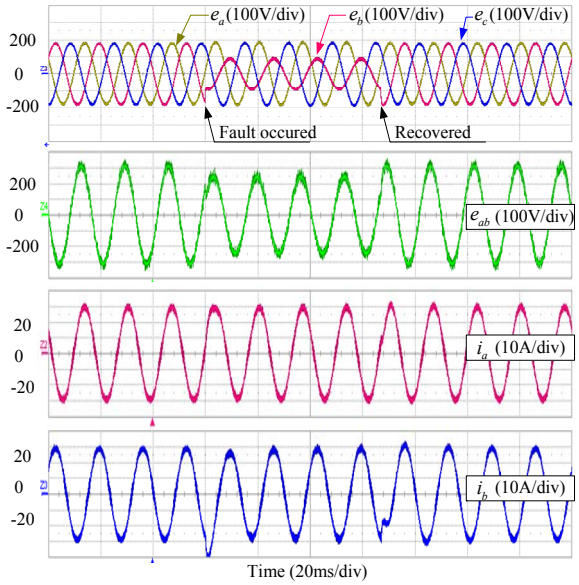


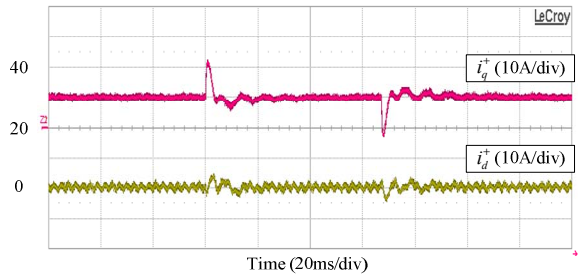
Fig. 8: Experimental setup with a back-to-back PWM converter configuration.

Table I: Parameters of the experiment system

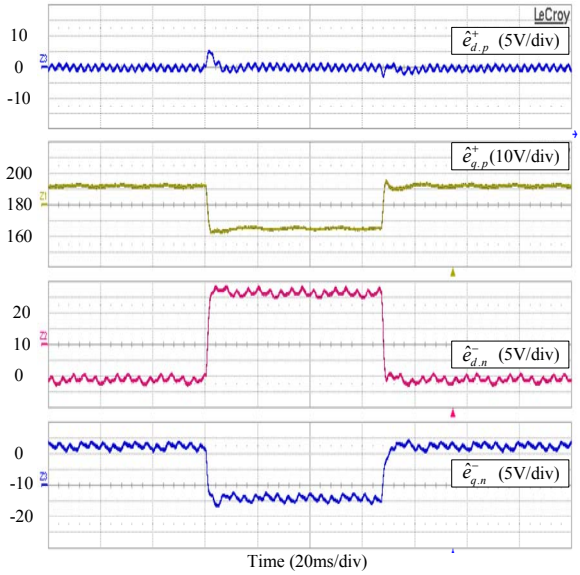
Grid Voltage	220Vrms/60Hz	DC-link Voltage	350V
Interface Inductor	1.5mH	DC-link Capacitor	3300μF
Switching Frequency	7kHz		



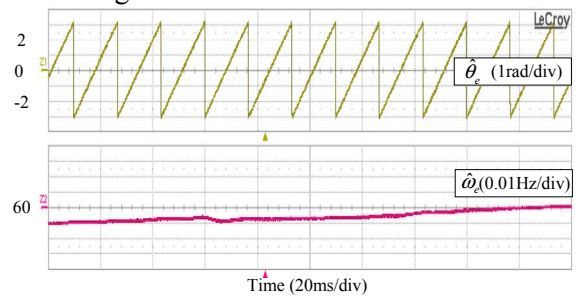
(a) Grid source voltages and line currents



(b) Synchronous *d-q* feedback current

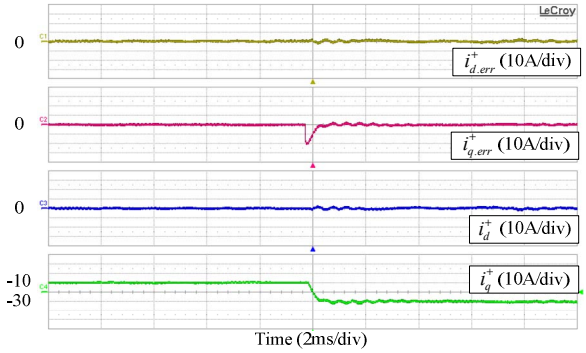


(c) Estimated positive and negative source voltage

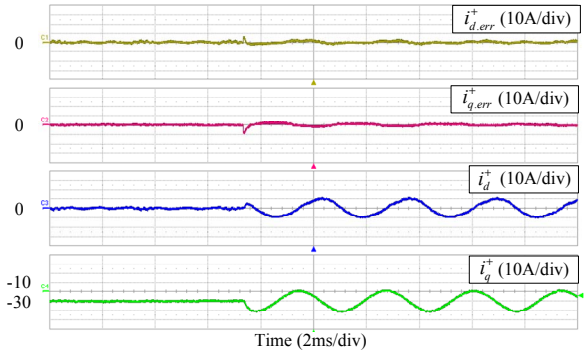


(d) Estimated grid angle and frequency

Fig. 9: Experimental result of current control and voltage estimation during the voltage sag.



(c) Step change of $i_{q.p}^{+*}$ from -10A to -30A



(d) Step change of $i_{q.n}^{-*}$ from 0A to -10A

Fig. 10: Experimental result of current control step response.

6. Conclusions

In this paper, a modified positive and negative sequence control scheme for the voltage sensorless PWM voltage source converter has been proposed and analyzed. Through the proposed current controller, current control performance has been improved without a strict separation between positive and negative sequence currents. Moreover, a positive and negative sequence source voltage observer has been designed to improve disturbance rejection and grid angle detection performance under source voltage unbalance. The feasibility of the proposed control scheme has been verified by simulation results. The experiment has been performed and presented to evaluate the transient response of the proposed control system under source voltage sag condition. It was concluded that fast current control performance and voltage estimation can be achieved by the proposed control scheme.

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