8th International Conference on Power Electronics - ECCE Asia
May 30-June 3, 2011, The Shilla Jeju, Korea

System Configuration and Control Strategy Using FPGA for Hybrid Vehicle Power Control Unit

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***Abstract*-- In this paper, it is presented a configuration to miniaturize HPCU (Hybrid vehicle Power Control Unit) and a control strategy using FPGA logic. To miniaturize the HPCU, the film capacitor is used as a DC-link capacitor instead of the electrolytic capacitor. Additionally, for the minimization of control hardware, a FPGA based controller is used to control multi-module of power converter. To verify the feasibility of the control strategy and FPGA based control hardware, the laboratory based load test is performed. With FPGA based hardware, the sampling frequency of the digital current control loop can be increased by 30% compared to DSP software based control system.**

***Index Terms*—Hybrid vehicle, FPGA, Power control, HPCU**

I. Introduction

Recently, hybrid electric vehicles (HEVs) have been developed intensively because of the increased cost of fossil fuel, and to decrease pollutant from emissions of internal combustion engine (ICE) [1]. Among the several types of HEVs, a series HEV can operate at optimal fuel efficiency point of ICE without degrading the dynamic performance [2] even though their integration results in more complexity than other types of HEV. In a series HEV, the reliability of the DC-link capacitor is the concern in the whole power converter of the HEV. In general, an electrolytic capacitor with large capacitance has been widely used as a DC-link capacitor because of higher energy density. However the electrolytic capacitor has poor reliability because it has low RMS currents capability, relatively high ESR (Equivalent Series Resistance). Also the electrolytic capacitor has short life span due to its inherent electrolyte. A metalized film capacitor is an alternative to the electrolytic capacitor, because it can withstand higher levels of surge voltage and RMS currents, and operate at relatively high temperature. Additionally, it has higher reliability than the electrolytic capacitor due to self-healing characteristics. Thus the metalized film capacitor might be the most suitable energy storage component in pulsed power system with harsh environment [3]-[5].

In many cases for HEVs control, a single DSP (Digital Signal Processor) has been used to control multi-module of power converter due to size and cost of control hardware. In these cases, a sampling frequency is constrained because of increased execution time for several current control loops. The constrained sampling frequency incurs control issues. In many hybrid vehicle applications, the torque and power density of the power train is one of the key factors to consider. Thus, to increase power density, the electric machines are usually designed with multi-pole and high speed ratings. In these cases, instability of current controller may occur because of high ratio of fundamental to sampling frequency if the sampling frequency is constrained [6]. To avoid above problem, FPGA (Field Programmable Gate Array) based control hardware might be more preferable for multi-module control than DSP based control hardware because the parallel execution of the control algorithm is inherently possible in FPGA based controller while only sequential processing is possible in DSP based controller [7][8].

This paper proposes a system configuration for HPCU employing the metalized film capacitor as a DC-link capacitor to increase the reliability of overall power system. The capacitance of a DC-link capacitor is reduced because of the characteristics of the metalized film capacitor which has higher RMS currents capability than the electrolytic capacitor at the cost of reduced density of capacitance. In this reason, the power control strategy focus on the suppression of a DC-link voltage fluctuation due to the small capacitance in a DC-link. Additionally, the FPGA based control is implemented in order to increase the sampling frequency of the current control loop and to minimize the hardware for the implementation of the control algorithm. Several tests based on the laboratory set-up have been made to verify the validity of proposed power control strategy and FPGA based control hardware.

II. Power System Configuration

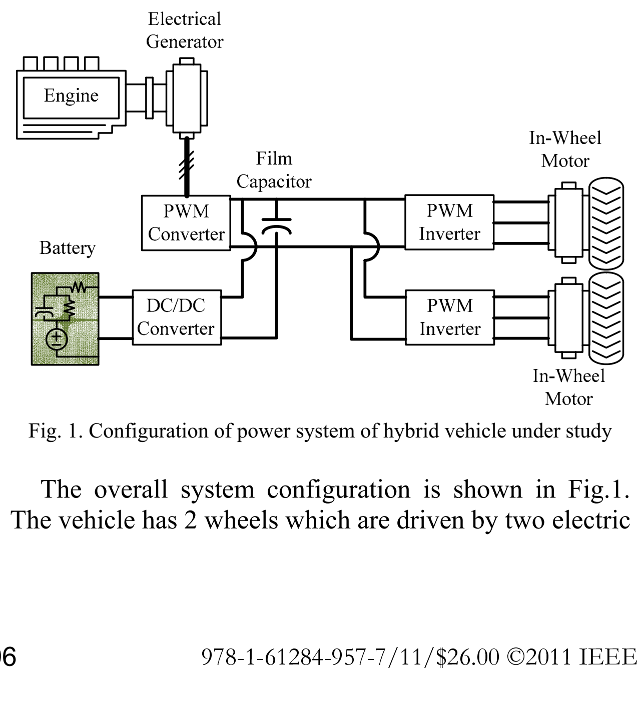

Fig. 1. Configuration of power system of hybrid vehicle under study

The overall system configuration is shown in Fig.1. The vehicle has 2 wheels which are driven by two electric

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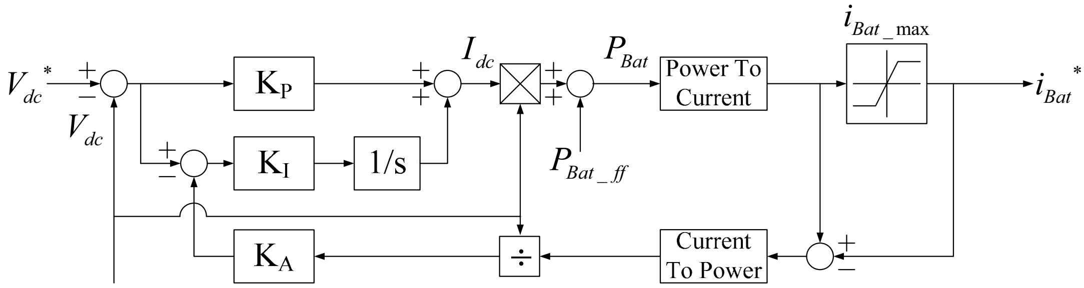

Fig. 2. Proposed voltage control method using battery power

machines independently. In addition, it has the engine generator as a main energy source which is interfaced with PWM boost rectifier and the battery as an energy storage element which is interfaced via DC/DC converter to DC-link. Because of two energy sources, it is possible that the DC-link voltage can be regulated regardless of the engine speed. Thus, it can be noted that the engine operating speed might move to the best fuel efficiency point at the demanded power. Due to the reduced DC-link capacitance of the metalized film capacitor, the initial charging circuit is saved and it further enhances the reliability of the overall system.

III. POWER CONTROL STRATEGY

The main objectives of power control strategy are as follows.

(1) Stable DC-link voltage regulation
(2) Maintaining optimal fuel efficiency
(3) Utilization of available maximum engine power

The regulation of the DC-link voltage should be achieved to guarantee the stable operation of the electrical machines used for in-wheel motor and for the engine generator. In the proposed system, the capacitance of the metalized film capacitor should be minimized to reduce the size and the cost of HPCU. Thus, the bandwidth of voltage regulator should be increased and the power fluctuation in the DC-link should be compensated instantaneously in order to regulate the DC-link voltage precisely. But the engine generator has slower dynamics than the load variation. So, it might not be possible to regulate the DC-link voltage using the engine generator only. In this paper, a power control strategy is proposed that the DC-link voltage is regulated by the battery and only the average load power is provided by the engine generator.

Fig. 2 depicts the voltage controller based on the battery which is interfaced via DC/DC converter to the DC-link. The power reference of the battery (P_{bat}), which is generated by voltage controller, is converted to the current reference of the battery (i_{bat}^*) using the battery voltage (V_{bat}). Because of the faster dynamic response of the battery power than that of the engine, the voltage fluctuation of the DC-link can be minimized in spite of reduced capacitance of the DC-link capacitor. To achieve the fast dynamic response of voltage controller, it is required to compensate the instantaneous power in the DC-link using the proper feed-forward power term. The feed-forward term can be calculated easily using the DC-link power balance equation.

$$P_{DC} = P_{load} - P_{gen} - P_{bat} \tag{1}$$

where P_{DC} : DC-link power, P_{load} : load power, P_{gen} : engine generator power and P_{bat} : battery power. P_{load} and P_{gen} can be calculated using simple power equation of electric machine.

$$P = \frac{3}{2}(v_{ds}^{r\,*} i_{ds}^r + v_{qs}^{r\,*} i_{qs}^r) \tag{2}$$

where $v_{ds}^{r\,*}$: d axis voltage reference, $v_{qs}^{r\,*}$: q axis voltage reference, $i_{ds}^{r\,*}$: measured d axis current and i_{qs}^r : measured q axis current, all at the rotor reference frame. It is obvious that the power in the DC-link capacitor should be zero to prevent the variation of the DC-link voltage. From (1), the feed-forward term (P_{bat_ff}) can be expressed by (3).

$$P_{bat\_ff} = P_{gen} - P_{load} \tag{3}$$

In the power control strategy, it is important utilizing the available maximum engine power to extend the lifetime of the battery as well as to enhance the efficiency of the overall power system. In order to maximize the engine power utilization while the voltage of the DC-link is regulated by the battery power, the current reference of the engine generator is calculated from the load power as shown in Fig. 3. The available maximum torque at the operating engine speed is always provided by dividing the load power by the engine speed.

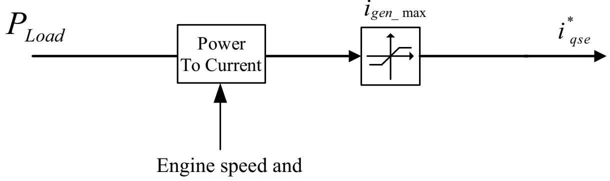

Fig. 3. Current reference generation of engine generator

In order for the engine to be operated at its optimal efficiency points for the overall load condition, the SFC (Specific Fuel Consumption) map is adopted [9]. As shown in Fig. 4, the engine speed reference (ω_{eng}^*) is given by SFC map from the load power. With these two algorithms, the engine can operate at the optimal fuel efficiency point and provide the available maximum power simultaneously.

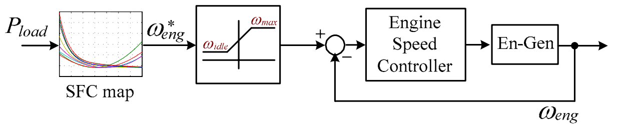

Fig. 4. Speed reference generation of engine generator

IV. Implementation of FPGA Based Controller

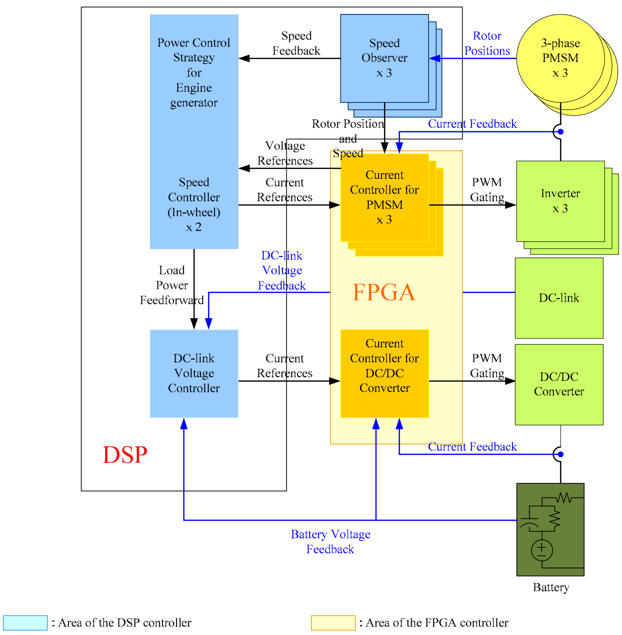

Fig. 5. Implemented scheme of the FPGA based controller

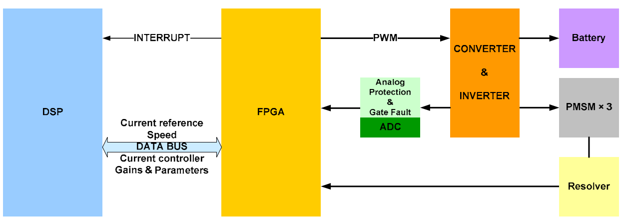

Fig. 6. Concept diagram of operation

Fig. 5 and Fig. 6 depict the block diagram of the FPGA based controller. With the FPGA hardware, four current control loops are implemented for driving the overall system. The proposed system has two in-wheel electric machines, one engine generator and one battery. Thus, the current controllers for 3-module of inverter and 1-module of DC/DC converter should be implemented. A DSP software acts as a role of host controller, where three speed observers to estimate the rotor speed of two in-wheel PMSMs (Permanent Magnet Synchronous Machines) and one PMSM as the generator are embedded. The current references for two in-wheel electric machines come from the speed controllers regulating speed of wheel. In addition, the current reference for the engine generator comes from the power control strategy which is used the calculated load power and estimated engine speed. Also, there is a DC-link voltage controller using the battery interfaced via DC/DC converter to the DC-link. As mentioned above, the current reference for the DC/DC converter comes from voltage controller. The load power is calculated from the feed-back currents and the gating signals of all power converters. Because not only current regulation loops but also PWM logics are implemented in FPGA hardware, the gating signals of all power converters, namely the PWM inverters for the two in-wheel electric machines, the inverter for the generator, and DC/DC converter, come from FPGA hardware, directly.

A. Implementation of current controller for PMSM

In this paper, the PI current regulator incorporating feed-forward decoupling method has been adopted as shown in Fig. 7, where ω_r, L_{dqs}, λ_{PM} and superscript '*' stand for rotor speed, synchronous inductance, back-emf constant, and reference of the variable, respectively. To implement the block of current controller in Fig. 7, the VHSIC Hardware Description Language (VHDL) has been used.

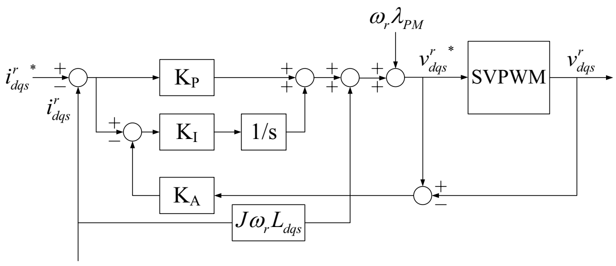

Fig. 7. Current controller for PMSM

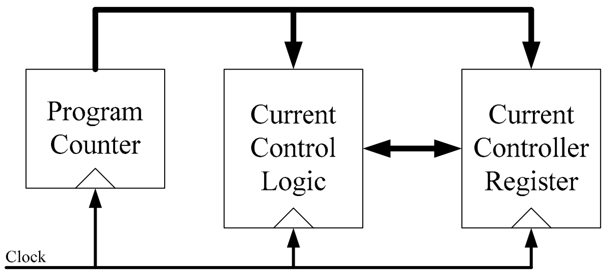

Fig. 8. Procedure of implemented current controller

TABLE I
PROCEDURE OF CURRENT CONTROL FOR PMSM

PC	Operation
0 ~ 3	a, b, c phase current measurement
4 ~ 7	Rotor reference frame transformation Anti-windup current calculation
8	Error calculation Flux linkage calculation
9 ~ 10	Calculation for P and I control
11	Feed-forward term calculation
12 ~ 13	Summation of PI controller's output and feed-forward term
14 ~ 22	Calculation for SVPWM
23 ~ 28	Anti-windup voltage calculation

The FPGA block of current controller has 3 stage of procedure as shown in Fig. 8. At first, the program counter's value is increased every one clock. And then, the logic block executes the each calculation for control at corresponding program counter. Simultaneously, the register stores the values of results of calculation at corresponding program counter. To implement the control logic, the fixed point calculation using Q Math has been adopted.

The calculation procedure for the current control loop can be divided by 3 processes. First, the reference frame transformation is necessary to apply vector control concept. Second, the calculations for PI control and feed-forward term is required. Finally, the calculations for SVPWM are carried out. The Look-Up Table (LUT) for trigonometric function is used for rotor reference frame transformation. Additionally, to enhance the performance of current controller, an anti windup function has been incorporated.

The operations of FPGA based current controller for the PMSM are described with corresponding program counter (PC) in Table I.

With 35 MHz clock frequency of FPGA and 29 clocks of program counter, total execution time of current regulation loop for the PMSM is 830 ns.

B. *Implementation of current controller for battery*

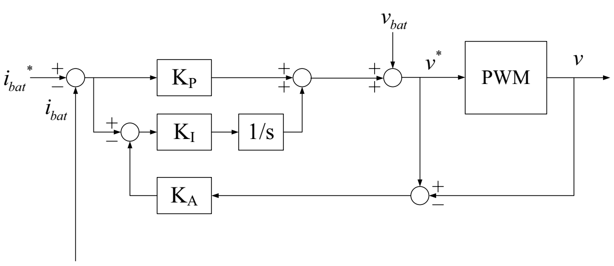

Fig. 9. Current controller for battery

Fig. 9 shows the current controller for battery. It has almost the same structure with AC current controller except on reference frame transformation. The operations of FPGA based current controller for the battery are also described with corresponding program counter (PC) in Table II.

TABLE II
PROCEDURE OF CURRENT CONTROL FOR BATTERY

PC	Operation
0 ~ 1	Battery current measurement
2 ~ 4	Anti-windup current calculation Error calculation
5 ~ 6	Calculation for P and I control
7	Feed-forward term calculation (battery voltage)
8	Summation of PI controller's output and feed-forward term
9	Calculation for PWM
10 ~ 11	Anti-windup voltage calculation

With 35 MHz clock frequency of FPGA and 11 clocks of program counter, total execution time of current controller for the battery is 315 ns.

V. SIMULATION RESULTS

To simulate the proposed power control strategy, the load condition and the power ratings of engine generator and in-wheel electric machines are assumed as follows.

The load power can be calculated from the mechanical parameters that are listed on Table III and motion equations that are given in (4)-(5).

TABLE III
MECHANICAL PARAMETERS OF VEHICLE

Parameters	Symbol	Value	Unit
Mass of Vehicle	m	1860	kg
Radius of Wheel	r	315	mm
Mass Factor	δ	1.05	None
Rolling Resistance	μ_r	0.02	None
Density of air	ρ	1.145	Kg/m^3
Drag Coefficient	C_d	0.3	Ns^2/m^4
Cross Section	A	2.16	m^2
Max Vehicle Speed	v	37	km/h
Acceleration time	t	2	s

$$F = \mu_r mg + 0.5\rho C_d Av^2 + \delta ma \qquad (4)$$

$$P = F \cdot v \qquad (5)$$

where, $F : force[N]$, $P : power[W]$, $v : velocity[m/s]$.

From the calculated load power, the parameters of the engine generator, the in-wheel electric machines and the battery have been designed as in Table IV.

TABLE IV
POWER RATINGS OF ELECTRIC MACHINES AND BATTERY

Parameters	Values
Engine rated power	86.2 kW
Engine idle speed	1600 r/min
Engine rated speed	3600 r/min
Engine generator rated torque	234 N-m
In-wheel electric machine	25 kW x 4 = 100 kW
Battery	10 kWh x 10C = 100 kW

A 1200 µF metalized film capacitor is installed in DC-link.

A. *Voltage control by the engine generator*

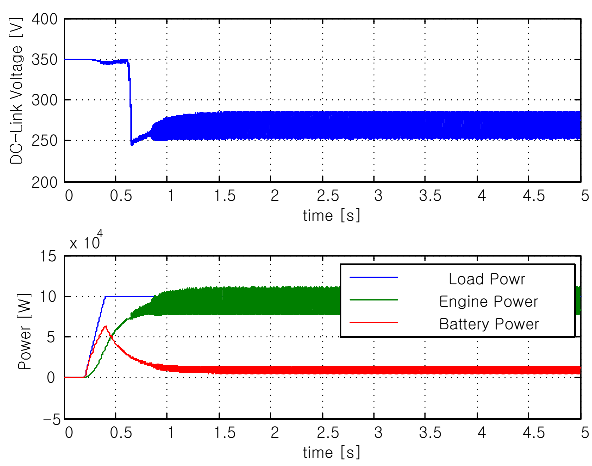

Fig. 10. Voltage control by the engine generator

Fig. 10 shows the simulation results of voltage control using engine generator. The DC-link voltage is regulated as 260 V. It means that the engine generator cannot regulate the DC-link voltage any more, and the stable operation of electric machines cannot be ensured. Aforementioned, the engine has slower dynamics than load variation. Thus, the integrator of voltage controller has limited values. Because the integrator of voltage controller compensates the error between the real load disturbance power and estimated load disturbance power which is used as feed-forward term of voltage controller, the integrator cannot compensate the error any more if the integrator has limited values which is saturation values. Therefore, as shown in Fig. 10, the voltage control method using the engine generator is not feasible with the low capacitance of DC-link.

B. *Voltage control by the battery (proposed algorithm)*

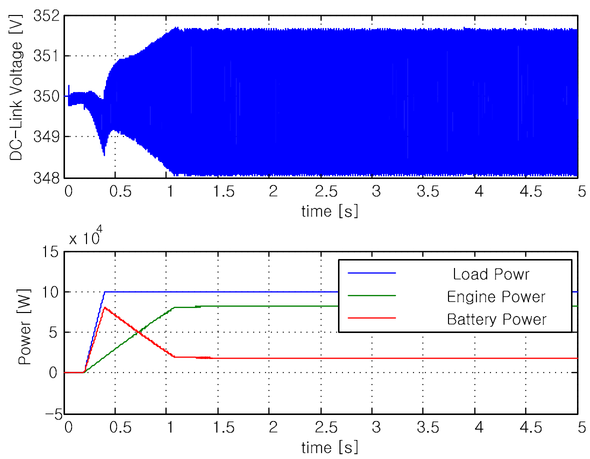

Fig. 11. Voltage control by the battery

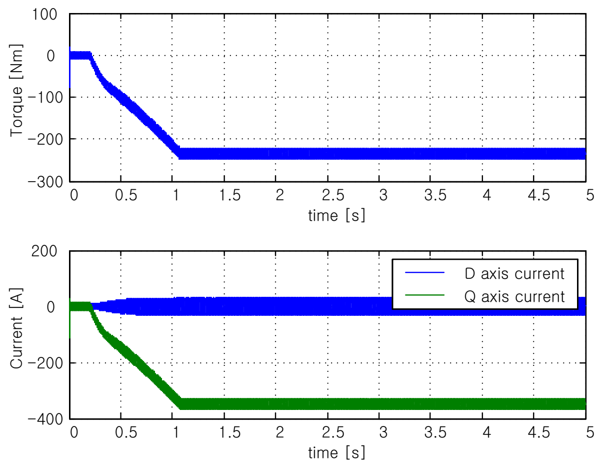

Fig. 12. Torque and current of engine generator

Fig. 11 shows the simulation results of voltage control using the battery. As a result of proposed power control strategy, the DC-link voltage is regulated within the tolerance range which can guarantee the stable operation of electric machines. The battery provides instantaneous power to regulate DC-link voltage. As the engine power is increased, it means that the engine speed increases, the battery power is decreased. Finally, after the engine speed reaches to its optimal speed, the battery provides only insufficient power which cannot be provided by the engine generator.

Fig 12 shows the torque and current of engine generator. After the engine speed reaches to its optimal speed corresponding with its load power, the engine generator outputs its maximum torque.

From the simulation results, it can be noted that the main objectives of power control strategies is achieved. As a consequence of the proposed power control strategy, the DC-link voltage regulation can be achieved within the tolerance range. Additionally, the engine can utilize its available maximum torque keeping the optimal fuel efficiency.

VI. Experimental Results

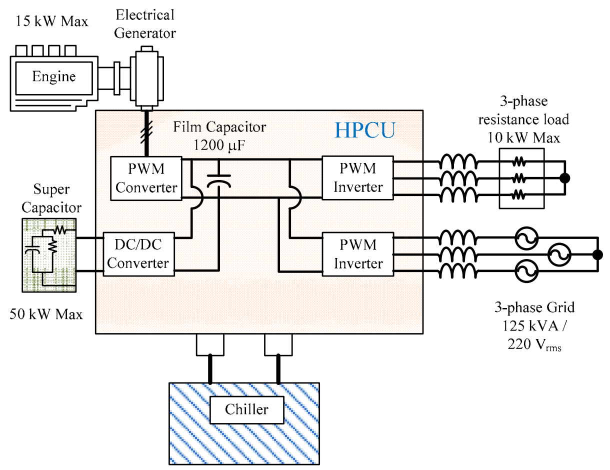

Fig. 13. Experimental setup for load test

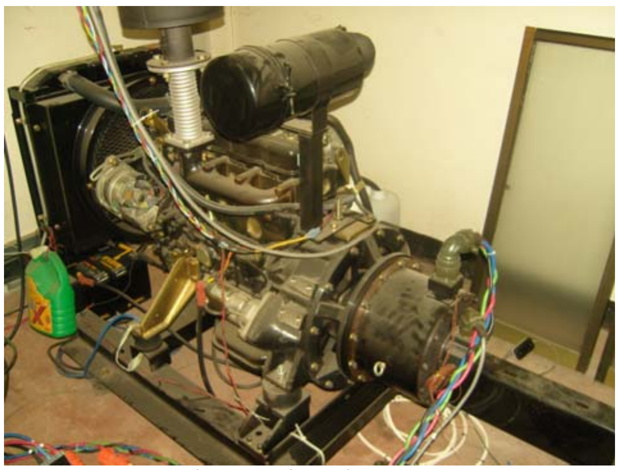

Fig. 14. Engine and generator

To verify the validity of the proposed power control strategy and implemented FPGA based control hardware, the load test based on the laboratory set-up was performed. The worst case scenario which has the load power slope with 5 (p.u.)/s has been simulated with dc-ac converters interfaced to the 3-phase grid and interfaced to the 3-phase resistance load. And the super capacitor was used to simulate the battery whose power capability is up to 50 kW. The engine has a rated power of 15 kW at maximum speed. To withstand the RMS current in the DC-link, a 1200 μF metalized film capacitor has been installed.

Fig. 15. Super capacitor

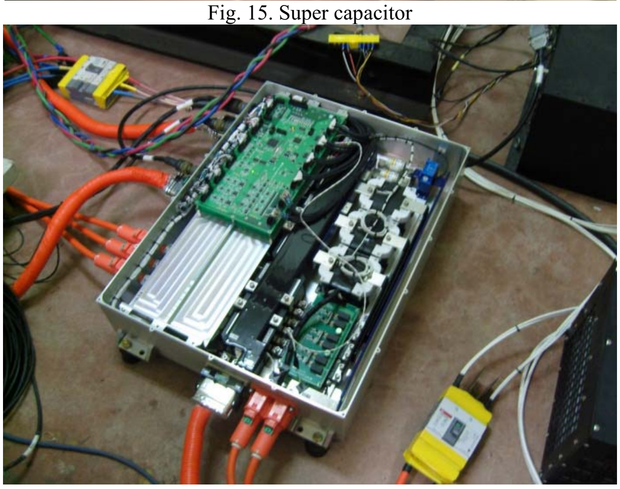

Fig. 16. Prototype HPCU

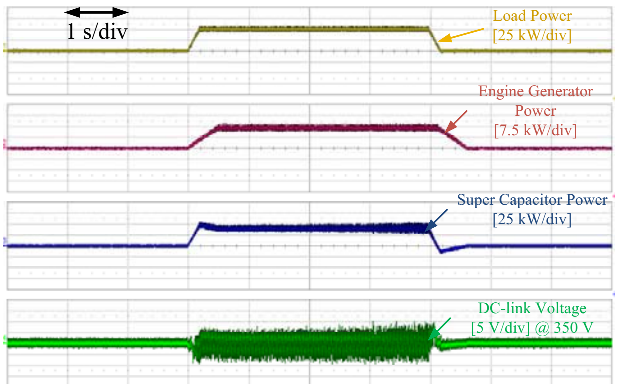

Fig. 17. Experimental result for the proposed control strategy

Fig. 17 shows the experimental results for the proposed power control strategy. As the load power increases, the engine power increases with the rate of the engine dynamic response. Thus, the battery (the super capacitor in laboratory experiment) supplies supplementary power not only in the transient state but also in the steady state. Hence, the DC-link voltage is well regulated within the tolerance range and the engine power is utilized maximally at its engine operating point.

Table V shows the comparison results of execution time of each control loop between DSP and FPGA. In the HPCU implemented, 20 kHz sampling frequency is possible in FPGA based controller whereas only 15 kHz sampling is possible in DSP based controller. This execution time difference would increases as the number of the modules increases. If the controller is implemented with 8 modules, the sampling frequency difference might be 7 kHz, which means that the sampling frequency of DSP based controller would be at best 8 kHz while that of FPGA based controller is 15 kHz.

TABLE V
COMPARISON OF EXECUTION TIME

	DSP	FPGA
ADC	3.8 μs	3.8 μs
DAC	6.8 μs	6.8 μs
Speed Observer	10.2 μs	10.2 μs
Measurement of current and voltage	2.4 μs	2.4 μs
D, q transformation and PWM time calculation	2.6 μs	0 μs
Voltage control	6 μs	8 μs
Current Control	31 μs	14.5 μs
Total execution time	62.4 μs	45.7 μs

VII. CONCLUSION

This paper has proposed a configuration to miniaturize HPCU (Hybrid vehicle Power Control Unit) and a control strategy using FPGA logic. Because the small metalized film capacitor is used as a DC-link capacitor, an instantaneous power control strategy is proposed that the voltage is regulated by the battery which has faster dynamic response than engine and the average load power is provided by the engine generator. Experimental results have been shown to verify the validity of the proposed control strategy based on the laboratory load tests. Also a FPGA based controller has been implemented to control multi-module of power converter in order to increase the sampling frequency and to minimize control hardware. The execution time has been compared between DSP based software controller and FPGA based hardware controller. It is expected that the effectiveness of FPGA would be further enhanced if more number of power modules should be controlled.

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