Parallel operation of PWM inverters for high speed motor drive system

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***Abstract*— This paper describes a topology with a parallel operation of PWM inverters for high speed motor drive systems. High speed motors have been widely used in industries to reduce system size and improve power conversion efficiency. However, the high speed motors sometimes suffer from core losses caused by PWM current ripples; noting that the phase inductance, L_s , of a high speed motor is smaller than that of ordinary motors, it is significant that the current ripple generated by a Pulse Width modulation(PWM) inverter becomes noticeable in the high speed motor. In the proposed topology, three PWM inverters are connected in parallel through nine coupled inductors. Compared to the PWM current ripple of the conventional single inverter system, that of the proposed scheme can be conspicuously reduced without the voltage drop at the inductors. In this paper, a theoretical analysis of the output voltage of the proposed topology is presented, and then the validity of the proposed method is verified by experimental results.**

I. INTRODUCTION

In some applications like turbo compressors and blowers, high speed motors have been used and it is directly coupled to the impeller. This structure has a number of merits compared to the conventional geared structure for high speed operation. It has smaller system size, better power conversion efficiency and lower maintenance cost due to the elimination of the gear box. Thanks to the advantages, the directly coupled structures with high speed motors become more popular in high power applications [1], [2] and their validities have been proved for years.

The high speed motors need higher fundamental frequency than ordinary motors. Since, however, the switching frequency of high power inverters is limited, parallel operations are needed in the high speed and high power applications. Besides, the high speed motors sometimes suffer from core losses caused by Pulse Width Modulation(PWM) current ripples; noting that the phase inductance, L_s , of high speed motors is smaller than that of ordinary motors, and the PWM current ripple of the high speed motor becomes larger [3].

Moreover, this problem becomes severe in high power applications. In order to reduce the current ripple, additional inductors can be connected between the inverter output and the motor terminal. In this configuration, however, voltage drop in the additional

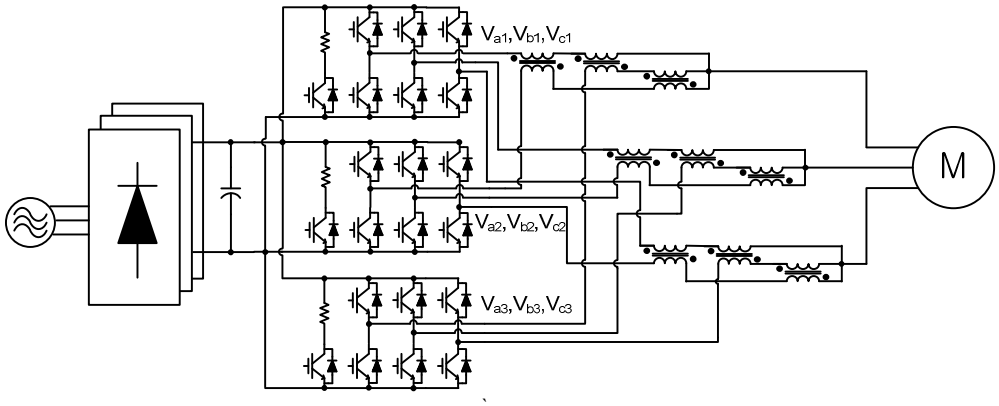


Fig.1 Proposed topology of parallel inverter with coupled inductor

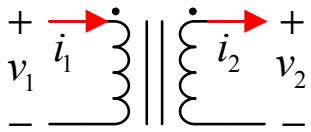


Fig. 2 Schematic diagram of coupled inductor

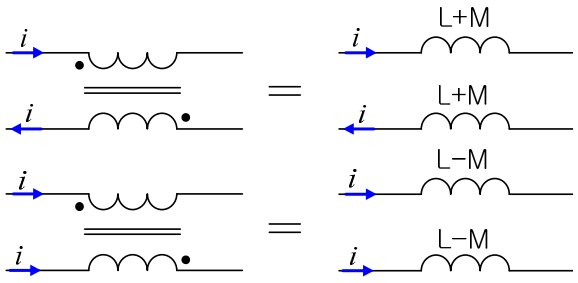


Fig. 3 Effective inductance of coupled inductor

inductors may be a problem.

In this paper, a topology for the parallel operation of PWM inverters is proposed to reduce the PWM current ripple. The proposed topology is shown in Fig. 1, where three PWM inverters are connected in parallel through nine coupled inductors. The diode rectifier in the figure may consists of many units to handle current capacity of the drive system In the proposed topology, the parallel inverters do the interleaving operation; the PWM carriers of the parallel inverters are shifted by 1/3 of the switching period away from each other. Thanks to the interleaving operation, the PWM current ripple of the motor can be conspicuously reduced. Moreover, because of the common mode operation of the coupled inductor, the fundamental currents of the machine are affected only by its leakage inductance, and the voltage drops of the coupled inductor are negligible while the coupled inductors reduce the circulating currents caused by the interleaving operation [4]. This is because the magnitude of the circulating currents depends on the differential mode inductance of the coupled inductor. A theoretical analysis of the output voltage of the proposed topology is also presented in this paper.

II. COUPLED INDUCTOR

Fig. 2 shows the schematic diagram of coupled inductor. v_1 , i_1 and v_2 , i_2 represent the voltage and current of first and secondary winding of coupled inductor and voltage equations can be described as (1).

$$v_1 = L\frac{di_1}{dt} - M\frac{di_2}{dt},\ v_2 = L\frac{di_2}{dt} - M\frac{di_i}{dt} \tag{1}$$

where L and M mean the self and mutual inductance of the coupled inductor, respectively. From this equation,

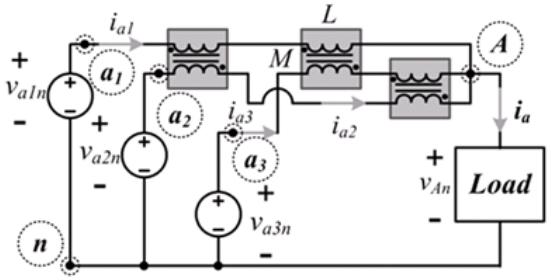


Fig. 4 Equivalent circuit

the effective inductance of the coupled inductor according to the direction of the flow of current can be derived.

As shown in Fig. 3, when currents flow in the opposite direction, the coupled inductor has the equivalent inductance as the sum of self and mutual inductance. On the other hand, the directions of current flow of the first and second winding are same, the coupled inductor equivalently act as leakage inductance which means the difference between the self inductance and mutual inductance. Using these characteristics of the coupled inductors, the proposed topology can minimize the effect of inductance for the fundamental current component, and maximize the effect of inductance for the ripple component of the circulation current due to interleaving operation.

III. ANALYSIS WITH EQUIVALENT CIRCUIT

A. *Small signal analysis*

Fig. 4 shows the per phase equivalent circuit of the proposed scheme. v_{a1n} , v_{a2n} and v_{a3n} mean pole voltages of the parallel inverters, and v_{An} means the equivalent pole voltage to the load. The relations between the pole voltages and output currents of inverters, i_{a1} , i_{a2} , and i_{a3} can be expressed as follows.

$$\begin{aligned} v_{a1n} - v_{An} &= 2L\frac{di_{a1}}{dt} - M\frac{di_{a2}}{dt} - M\frac{di_{a3}}{dt}, \\ v_{a2n} - v_{An} &= 2L\frac{di_{a2}}{dt} - M\frac{di_{a1}}{dt} - M\frac{di_{a3}}{dt}, \\ v_{a3n} - v_{An} &= 2L\frac{di_{a3}}{dt} - M\frac{di_{a1}}{dt} - M\frac{di_{a2}}{dt}. \end{aligned} \tag{2}$$

Since the voltages and the currents have two frequency components, which are a fundamental frequency of the motor and a PWM switching frequency of each inverter, (2) can be rewritten as follows.

$$
\begin{aligned}
&\hat{v}_{a1n}+\tilde{v}_{a1n}-\left(\hat{v}_{An}+\tilde{v}_{An}\right)\\
&=2L\frac{d}{dt}(\hat{i}_{a1}+\tilde{i}_{a1})-M\frac{d}{dt}(\hat{i}_{a2}+\tilde{i}_{a2})-M\frac{d}{dt}(\hat{i}_{a3}+\tilde{i}_{a3}),\\
&\hat{v}_{a2n}+\tilde{v}_{a2n}-\left(\hat{v}_{An}+\tilde{v}_{An}\right)\\
&=2L\frac{d}{dt}(\hat{i}_{a2}+\tilde{i}_{a2})-M\frac{d}{dt}(\hat{i}_{a1}+\tilde{i}_{a1})-M\frac{d}{dt}(\hat{i}_{a3}+\tilde{i}_{a3}),\\
&\hat{v}_{a3n}+\tilde{v}_{a3n}-\left(\hat{v}_{An}+\tilde{v}_{An}\right)\\
&=2L\frac{d}{dt}(\hat{i}_{a3}+\tilde{i}_{a3})-M\frac{d}{dt}(\hat{i}_{a1}+\tilde{i}_{a1})-M\frac{d}{dt}(\hat{i}_{a2}+\tilde{i}_{a2})
\end{aligned}
\tag{3}
$$

where '^' means the components of the fundamental frequency and '~' means those of the PWM frequency. Considering two frequencies, the equations of the fundamental and PWM frequency component can be derived as (4) and (5), respectively.

$$
\begin{aligned}
\hat{v}_{a1n}-\hat{v}_{An}&=2L\frac{d\hat{i}_{a1}}{dt}-M\frac{d\hat{i}_{a2}}{dt}-M\frac{d\hat{i}_{a3}}{dt},\\
\hat{v}_{a2n}-\hat{v}_{An}&=2L\frac{d\hat{i}_{a2}}{dt}-M\frac{d\hat{i}_{a1}}{dt}-M\frac{d\hat{i}_{a3}}{dt},\\
\hat{v}_{a3n}-\hat{v}_{An}&=2L\frac{d\hat{i}_{a3}}{dt}-M\frac{d\hat{i}_{a1}}{dt}-M\frac{d\hat{i}_{a2}}{dt}.
\end{aligned}
\tag{4}
$$

$$
\begin{aligned}
\tilde{v}_{a1n}-\tilde{v}_{An}&=2L\frac{d\tilde{i}_{a1}}{dt}-M\frac{d\tilde{i}_{a2}}{dt}-M\frac{d\tilde{i}_{a3}}{dt},\\
\tilde{v}_{a2n}-\tilde{v}_{An}&=2L\frac{d\tilde{i}_{a2}}{dt}-M\frac{d\tilde{i}_{a1}}{dt}-M\frac{d\tilde{i}_{a3}}{dt},\\
\tilde{v}_{a3n}-\tilde{v}_{An}&=2L\frac{d\tilde{i}_{a3}}{dt}-M\frac{d\tilde{i}_{a1}}{dt}-M\frac{d\tilde{i}_{a2}}{dt}.
\end{aligned}
\tag{5}
$$

B. common mode operation of coulpled inductor

Since all inverters have same voltage references to regulate output current and the impedances of the coupled inductors are balanced, voltages and currents equations of the fundamental component can be described as (6) and (7). From them, (4) can be rewritten as (8).

$$
\hat{v}_{a1n}=\hat{v}_{a2n}=\hat{v}_{a3n}. \tag{6}
$$

$$
\hat{i}_{a1}=\hat{i}_{a2}=\hat{i}_{a3}=\frac{1}{3}\hat{i}_{a}. \tag{7}
$$

$$
\hat{v}_{a1n}-\hat{v}_{An}=\frac{2}{3}(L-M)\frac{d\hat{i}_{a}}{dt}. \tag{8}
$$

Generally, the leakage inductance of a coupled inductor is much smaller than the mutual inductance. So, (8) means that the voltage drops of the fundamental frequency currents on the coupled inductors would be negligible .And, it is possible to reduce the current ripples without fundamental component voltage drop by the coupled inductors.

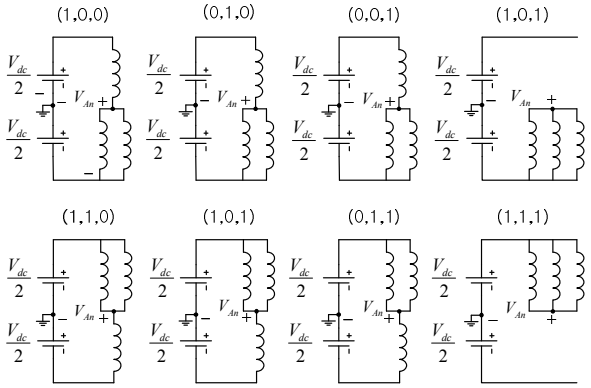


Fig. 5 Equivalent circuit according to switching state

C. Differential mode operation of coupled inductor

Instantaneous pole voltage differences due to the interleaving operation of the paralleled inverter result in circulating currents through the inverters. And, the common dc-link are return path of these circulating currents. The voltage differences can be expressed using (5) as follows.

$$
\tilde{v}_{a1n}-\tilde{v}_{a2n}=\left(2L+M\right)\frac{d}{dt}\left(\tilde{i}_{a1}-\tilde{i}_{a2}\right). \tag{9}
$$

The circulating current can be suppressed by a coupled inductor whose equivalent inductance is (2L+M). And, the circulating current can be reduced conspicuously.

D. Output voltage with interleaving operation

In a single inverter system, only two kinds of pole voltages, $-V_{dc}/2$ and $V_{dc}/2$ are available. In the proposed topology with three inverters, however, the pole voltage has four voltage levels due to the parallel operation of inverters under the assumption that the impedances of the coupled inductors are balanced. Fig. 5 shows per phase equivalent circuits of the proposed topology according to switching states, and the output pole voltage of each state are listed as in Table I.

Four kinds of pole voltages, $-V_{dc}/2$, $-V_{dc}/6$, $V_{dc}/6$, $V_{dc}/2$ can be used to synthesize the output voltage using the proposed topology. Combining these pole voltages, output line-line voltage, V_{AB} has seven voltage levels, namely, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, 0, $V_{dc}/3$, $2V_{dc}/3$, V_{dc}.

Table I Output pole voltage

State	S_{a1}, S_{a2}, S_{a3}	V_{An}
0	(0, 0, 0)	$-V_{dc}/2$
1	(0, 0, 1)	$-V_{dc}/6$
2	(0, 1, 0)	$-V_{dc}/6$
3	(1, 0, 0)	$-V_{dc}/6$
4	(0, 1, 1)	$V_{dc}/6$
5	(1, 0, 1)	$V_{dc}/6$
6	(1, 1, 0)	$V_{dc}/6$
7	(1, 1, 1)	$V_{dc}/2$

Table II Parameters of coupled inductor

Relative permeability of core	125
Number of turns	12
Self inductance	56.0 μH
Mutual inductance	55.5 μH

Therefore, the output voltage of the proposed topology could have much less harmonic contents compared to harmonics of the single inverter. In result, the proposed method can reduce current ripples of the output current furthermore.

IV. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed method, some experiments were carried out. The experimental configuration is shown as Fig. 6. Fig. 6(a) shows a proto type coupled inductor with the high-flux core material and Litz wire. The parameters of the inductor measured by an RLC meter are listed as Table II. It can be noticed that the leakage inductance is less than 1 % of the self inductance of the coupled inductor.

Table III Parameters of induction machine

Rated power	22 kW
Rated voltage	220 V
Rated current	74.6 A
Rated speed	1765 r/min
Pole	4

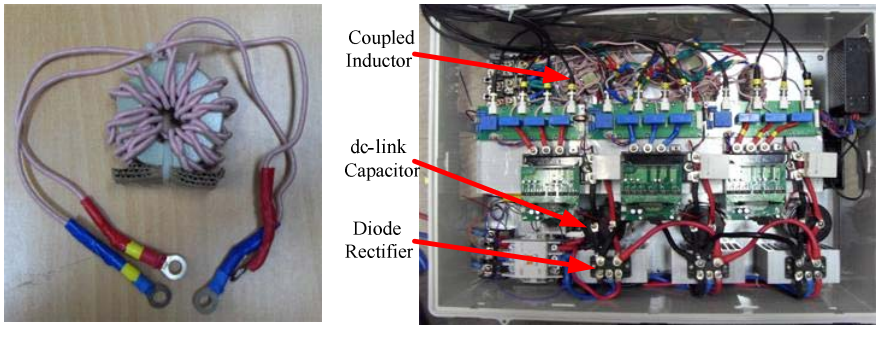
Table IV Operating condition

Input voltage(line-to-line rms)	220 *V*
Operating speed	1,000 *r/min*
Switching frequency	10 *kHz*
Sampling frequency	20 *kHz*
Output power	3 *kW*

With these coupled inductors, a prototype inverter system was implemented as shown in Fig. 6(b). The system consisted with three inverters, and three diode rectifier units connected in parallel and nine coupled inductors according to the proposed circuit arrangement as shown in Fig. 1.

An induction motor was driven with the proposed inverter system and a DC machine was used as a load. Parameters of the induction machine are listed in Table III. Operating condition of the induction machine is shown as in Table IV.

Under this condition, experiments with two kinds of inverter systems were performed. One is a single inverter system and the other is the proposed one. The phase currents of the induction machine and their FFT (Fast Fourier Transform) results of two cases were demonstrated as in Fig. 7(a) and (b), respectively. When the induction machine was driven with the single PWM inverter, the phase current of the motor has some



(a) (b)

Fig. 6 Experimental setup;
(a) coupled inductor and (b) proto type inverter system

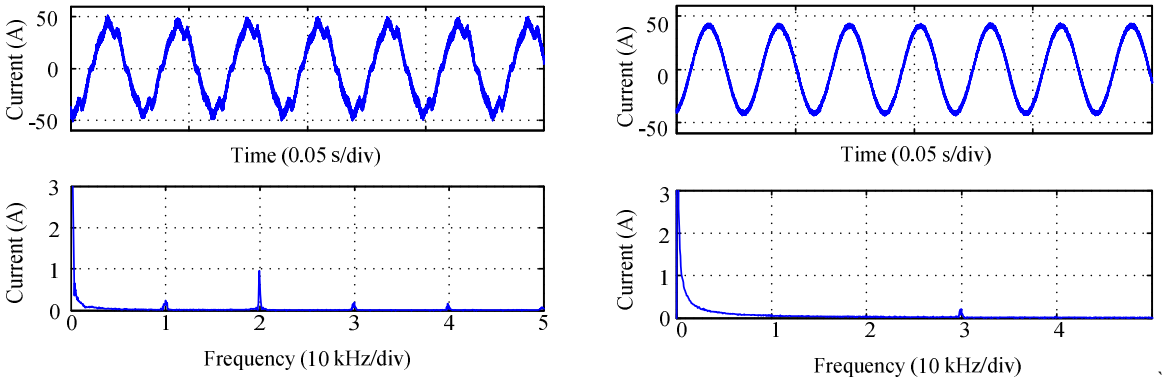


Fig. 7. Motor phase current and FFT waveforms
(a) wth single PWM inverter, (b) with proposed topology

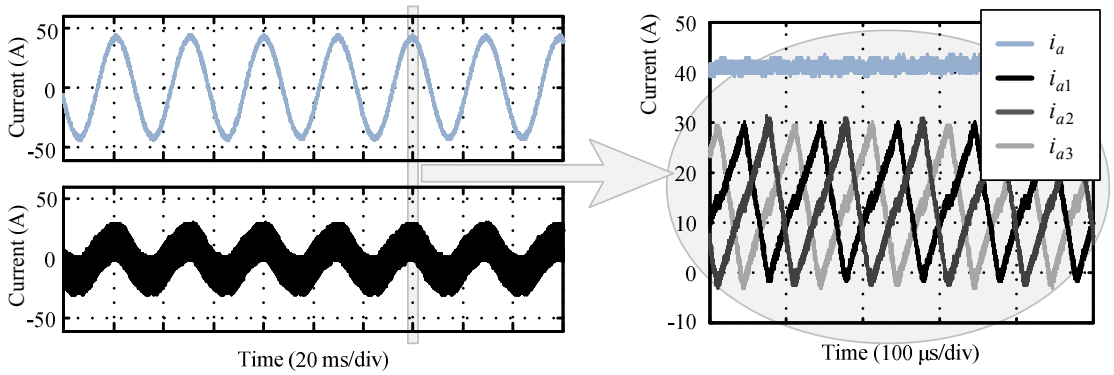


Fig. 8. Current waveforms of proposed topology
(a) waveforms of motor phase current, i_a , and inverter output current i_{a1}
(b) zoom-in waveforms of Fig. 8 (a) including i_{a2} and i_{a2}

distortions and the FFT waveform shows that ripple currents is quite large.

When the proposed topology is used to drive induction machine under the same condition as the previous one, the phase current of the motor are shown as shown Fig. 7(b). The current waveform has no distortion and its FFT result shows that PWM frequency component of the phase current is remarkably reduced. This experimental result clearly demonstrate that the proposed topology has advantage in reducing PWM current ripple compared over a single PWM inverter system.

The waveforms of the motor phase current, i_a , and the output currents of each parallel inverters, i_{a1} , i_{a2} and i_{a3} are displayed in Fig. 8(a). And, Fig. 8(b) shows the zoom-in waveform of the Fig. 8(a). The output currents of three inverters have the ripple of about 30 A and waveforms of currents are shifted 1/3 of the switching frequency away from each other due to interleaving operation. Thanks to the interleaving operation, the resultant motor current, which is the sum of output currents of three inverters, has significantly reduced ripples.

Fig. 9 shows the waveforms of the circulating currents, which flow through the inverters. Fig. 9(a) and (b) show that the current when output powers are 0 kW and 3 kW, respectively. Both of them show similar waveforms regardless of output powers. This is because the currents come from the instantaneous voltage difference between inverters and it does not depend on the output power. The magnitude of the circulating currents can be estimated by (9) and expressed as follows.

$$i_{cir} = \frac{V_{dc}}{2\pi f_{sw}(2L+M)} \approx 31.1 \qquad (10)$$

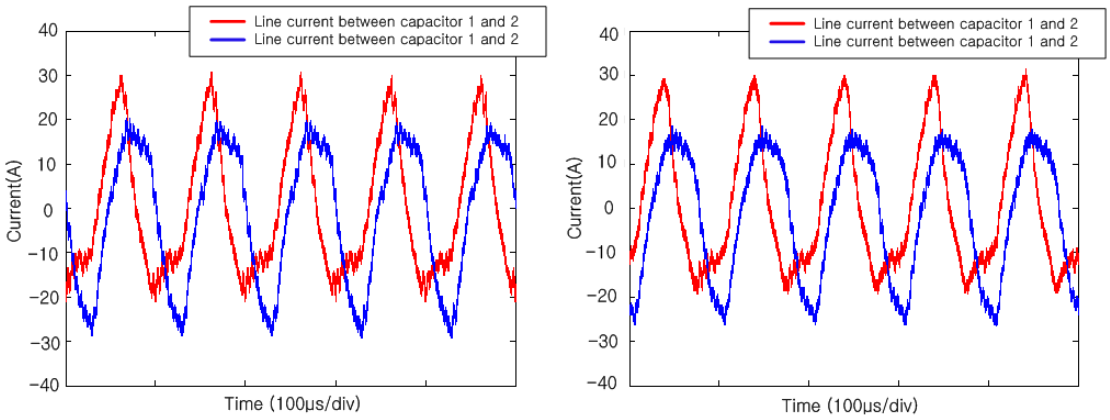


Fig 9 Line current between dc-link capacitors
(a) Output power 0 kW and (b) Output power 3kW

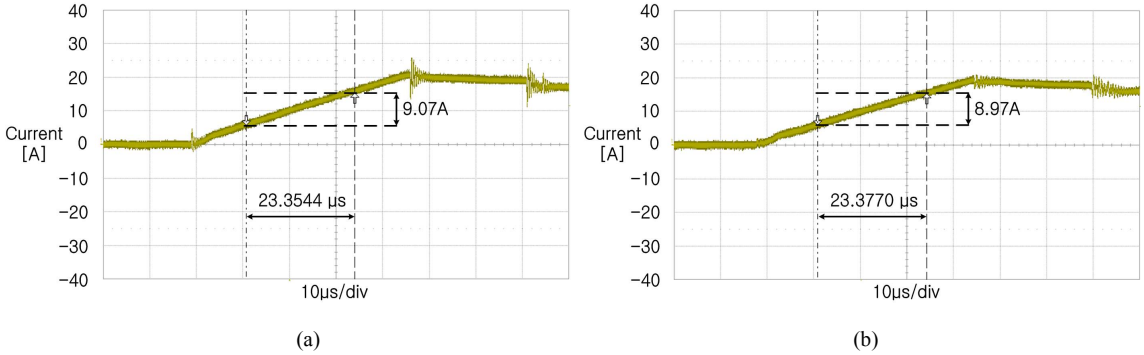


Fig. 10. Current waveform of the motor when apply`ing a step voltage;
(a) with single PWM inverter and (b) with proposed topology

Table V Measured inductance

	Single inverter	Proposed topology
Δt	23.4 μs	23.4μs
Δi	9.1 A	9.0 A
L_σ	514 μH	520 μH

From Fig 9, it can be seen that the magnitude of the circulating current is almost same to the estimated value by (10). This means that the magnitude of the circulating currents is determined based on the voltage equation of (9) and the currents can be reduced by the value of the coupled inductors in (9).

In order to evaluate the voltage drop on the additional coupled inductors, the output inductance of the load including coupled inductors was measured with the single PWM inverter and the proposed scheme. The inductance was measured by applying a pulse voltage to the input terminal of motor including coupled inductors and measuring the output current as shown in Fig. 10.

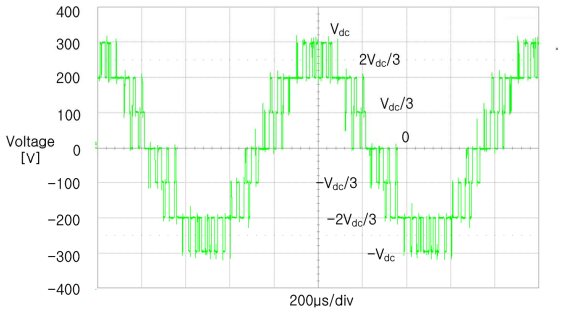


Fig. 11 Output line voltage of proposed topology

The measured inductances with two systems are listed in Table V.

The difference of the measured inductance between two cases is about 6 μH. The difference may come from leakage inductances of the coupled inductors and parasitic inductances of wiring cables. The additional inductance due to the coupled inductor is negligible. Therefore, it can be concluded that the proposed method can reduce the ripple current with negligible voltage

drop.

Fig. 11 shows the output line-line voltage, V_{AB} when the reference is a sine wave whose magnitude is 150 V and frequency is 1 kHz. As mentioned before, the proposed topology has seven levels of line-line output voltage, and the output current ripple can be reduced furthermore by these multilevel output voltages.

V. CONCLUSIONS

This paper describes a topology with a parallel operation of PWM inverters for high speed motor drive systems. In the proposed topology, three PWM inverters are connected in parallel through nine coupled inductors. Thanks to the interleaving operation of parallel inverters, the current ripples are remarkably reduced compared to that of single PWM inverter systems. On the other hand, the voltage drops on the coupled inductor are negligible due to the common mode operation of the coupled inductor. And, the coupled inductors also reduce the circulating currents caused by the interleaving operation. The output voltage of the proposed topology is analyzed and the feasibility is also verified experimentally.

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