Analysis on Output LC Filters for PWM Inverters

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Abstract-The cutoff frequency of output LC filters of PWM inverters limits the control bandwidth of the converter system while it attenuates voltage ripples caused from the inverter switching. For a selected cutoff frequency of an output LC filter, infinite number of L-C combinations is possible. This paper analyses the characteristics of output LC filters for PWM inverters in the view of L-C combinations. Practical circuit conditions such as no-loads, full resistive-loads, and inductive-loads are considered in the analysis. This paper proposes a design criterion and a design example for the L-C filter combination considering both the control performance and the size of PWM inverters. An experimental PWM inverter system based on the proposed output LC filter design guideline is built and tested.

Key words: PWM inverter, output LC filter, cut-off frequency, L-C combination, inverter size.

I. INTRODUCTION

PWM inverters are widely used in modern power electronics, such as adjustable speed drives (ASD), active power filters (APF), dynamic voltage restorers (DVR), or uninterruptible power supplies (UPS), etc.

Passive LC filters are commonly used on ac terminals of PWM inverters when the output voltages of inverter systems are main control target. The main purpose of the output LC filter is attenuating voltage ripples came from the inverter switching. The attenuation effect can be increased by decreasing the filter cut-off frequency against the switching frequency of inverters according to $-40\log(f_{sw}/f_{cutoff})$.

However, the control bandwidth of inverter systems is limited by the filter cut-off frequency [1]. Increasing the control bandwidth is important not only for a fast operation of inverter systems but also for exact voltage compensation without phase delay [2][3][4]. Thus, there is a trade-off between the attenuation effect and the control band width in LC filter design.

Besides after deciding the filter cut-off frequency on LC filters, two more problems may occur. One problem is voltage oscillations. Very large voltage over shoot may occur at the filter capacitor when inverters respond to almost step manner at transient state. The voltage over shoot can be damped out by generating a damping voltage that is negatively proportional to the filter capacitor current [1][5]. This is called active damping.

The other problem is large amount of transient current that flows through the inverter ac terminals when inverters must generate a quite large amount of voltages suddenly. When the transient current goes over certain limitation, the control system should decrease the current by reducing the inverter voltage instantly. Otherwise, the inverter system may be tripped by over current fault.

However, when the inverter voltage is instantly reduced by the current protection, the active damping may not work properly so that the output voltage may severely oscillate in the transient state. This problem may be solved by over sizing the inverter, which inevitably results in cost issues. This paper proposes LC filter design guideline that minimizes the transient over current without loss of active damping performance of inverter systems.

There are infinite combinations of filter inductance and filter capacitance for a given filter cutoff frequency. Intuitively, the transient current of a PWM inverter may be decreased when the filter inductance increases. However, the output ac voltages become more sensitive on the load current disturbance because of comparatively small value of the filter capacitance. Moreover, large filter inductors not only increase the cost and weight of the output filters but also increase voltage stress on the inverter switches, since the voltage drop of the inductor results in the loss of inverter output voltage.

This paper analyses the characteristics of output LC filters for PWM inverters in the view of the L-C combinations. Practical circuit conditions such as no-loads, full resistive-loads, and inductive-loads are considered in the analysis. Based on the analysis, a novel filter design guideline that guarantees good control dynamics with a minimum inverter size is proposed. Proposed theory is verified by an experimental set up.

II. ANALYSIS ON PWM INVERTER SYSTEM

The single phase equivalent circuit of inverter systems can be described by Fig.1. In Fig. 1, V_{INV} is the inverter output voltage, L_f is the filter inductor, C_f is the filter capacitor, and R_f is the series equivalent resistance existed in the filter inductor and inverter switches.

Fig.2 shows a single phase equivalent circuit for a properly controlled PWM inverter system. The output regulating voltage V_{Com} regulates the ac terminal voltage of

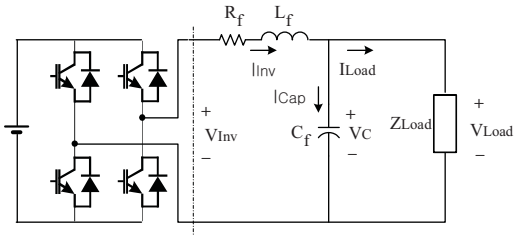


Fig. 1 Single phase equivalent circuit of PWM inverter system.

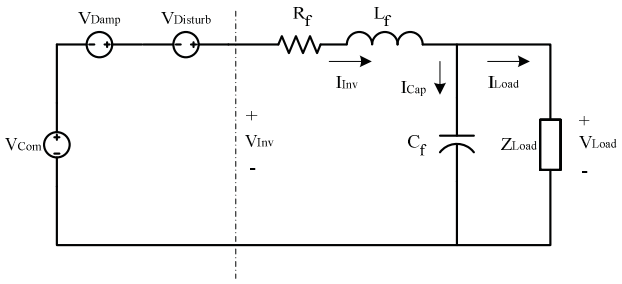


Fig. 2 Single phase equivalent circuit of properly controlled inverter system.

a PWM inverter to a reference voltage. The oscillation damping voltage V_{Damp} damps out the overshoot of the output voltage. The disturbance rejection voltage $V_{Disturb}$ suppresses the voltage disturbance occurred from load current. If the PWM inverter system is controlled properly, then the three controlled voltages can be generated by the inverter controller as follows.

A. Output Regulating Voltage

The output regulating voltage V_{Com} regulates the output terminal voltage of a PWM inverter system. When the oscillation damping voltage V_{Damp} and the disturbance rejection voltage $V_{Disturb}$ are ideally controlled, then the load current disturbance may be completely decoupled and the system damping factor becomes unity so that the output LC filter acts just as a time delay component with a delay time of $2/\omega_f$ in the steady state.

Thus the instantaneous load voltage V_{Load} can be regulated exactly to the reference load voltage V_{Load}^* when the time delay is pre-compensated by (1) in the steady state.

$$V_{Com} = (1+\frac{2}{\omega_f}s)V_{Load}^* . \tag{1}$$

where, $\omega_f = \frac{1}{\sqrt{L_f C_f}}$: filter cut-off frequency.

B. Oscillation Damping Voltage

The damping coefficient can be increased electronically by generating the oscillation damping voltage V_{Damp} as (2).

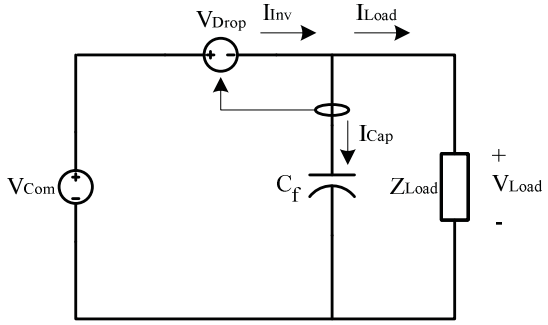


Fig. 3 Single phase equivalent circuit of PWM inverter system represented by two controlled voltage sources.

$$V_{Damp} = K_{Damp} \times i_{Inv} = -aR_f \times i_{Inv} . \tag{2}$$

According to (2), V_{Damp} is proportional to the inverter current with negative coefficient $K_{Damp} = -aR_f$. Thus, the oscillation damping voltage V_{Damp} acts as a series resistance adding to the R_f which results in a total equivalent resistance of $(1+a)R_f$ in series to the filter inductor L_f. Thus, the effective system damping factor ξ_c can be increased as (3).

$$\begin{aligned} \xi_c &= (1+a)\frac{R_f}{2}\sqrt{\frac{C_f}{L_f}} \\ &= (1+a)\xi_f \end{aligned} \tag{3}$$

Therefore, the control gain of the oscillation damping voltage $K_{Damp} = -aR_f$ to achieve desired damping factor is determined by (4).

$$K_{Damp} = -aR_f = R_f - 2\xi_c\sqrt{\frac{L_f}{C_f}} . \tag{4}$$

C. Disturbance Rejection Voltage

Since the oscillation damping voltage V_{Damp} affects to increase the equivalent series resistance of the PWM inverter ac terminal, the output load voltage may be deviated from the output regulating voltage V_{Com} by the load current. The magnitude of the load voltage decreases and the phase of the load voltage shifts from the output regulating voltage V_{Com} when the load is reactive. When the load current is non-sinusoidal, the output load voltage may be further distorted by the voltage drop across the equivalent series resistance $(1+a)R_f$ and the filter inductance L_f. The disturbance rejection voltage $V_{Disturb}$ should be generated by (5) to get rid of the voltage distortion due to the load current disturbance.

$$V_{Disturb} = \left[(1+a)R_f + sL_f\right] \times i_{Load} . \tag{5}$$

D. Equivalent Voltage Drop

The total voltage drop, occurred from the oscillation damping voltage V_{Damp} and the disturbance rejection voltage $V_{Disturb}$, can be calculated by (6).

$$\begin{aligned} V_{Drop} &= (R_f + sL_f)\times i_{Inv} - (V_{Damp} + V_{Disturb}) \\ &= \left[(1+a)R_f + sL_f\right]\times(i_{Inv} - i_{Load}) \\ &= \left[(1+a)R_f + sL_f\right]\times i_{Cap} \end{aligned} \quad . \qquad (6)$$

Here, the equivalent voltage drop V_{Drop} of a properly controlled PWM inverter system is only determined by the filter capacitor current. Thus the single phase equivalent circuit of the PWM inverter system shown in Fig.2 can be simplified by Fig.3. Here, sL_f can be neglected since $(1+a)R_f >> sL_f$, where $\omega < \omega_f$ in most practical cases. The equivalent voltage drop V_{Drop} causes an error to the reference load voltage.

III. Analysis On Output LC Filter

The peak value of inverter output current is important factor in designing the inverter size. The inverter current rating is normally determined by the filter impedance and the load impedance in the steady state. However, in the transient state where the inverter should synthesize output voltage rapidly, the instantaneous inverter current may exceed the rated peak value because of the LC filter circuit.

When the transient current of a PWM inverter goes over the rated peak value, it must be limited by adjusting the inverter output voltage to protect inverter itself from over current fault. In this case, the control dynamics of the output voltage is badly affected by the transient current.

Conventionally, this transient current problem was compensated by over sizing the inverters. This paper proposes design guideline of LC output filters that do not generate the transient current problem without increasing the inverter size.

A. Equivalent Circuit With No Load

Fig.4 shows a simplified equivalent circuit of a PWM inverter system without a load. In worst case, the reference load voltage V_{Load}^* is commanded by the peak value of $\sqrt{2}V$, where V is the rated rms voltage. Since major problems occur in very short time, this paper focuses on the transient state analysis for the inverter system. Thus the reference load voltage V_{Load}^* can be regarded as dc value during the transient state. In the figure, aR_f is the equivalent resistance by the oscillation damping control V_{Damp}. Various voltage control methods for compensating the time delay of the output LC filters have been exploited since the phase delay compensation described by (1) based on a lead-lag controller no more works in the transient state. However, this paper uses a simple feed forward controller for the output voltage regulation, ie. $V_{Load}^* = V_{Com} = \sqrt{2}V$ for a simplicity, since developing the output voltage controller itself is not the scope of this paper.

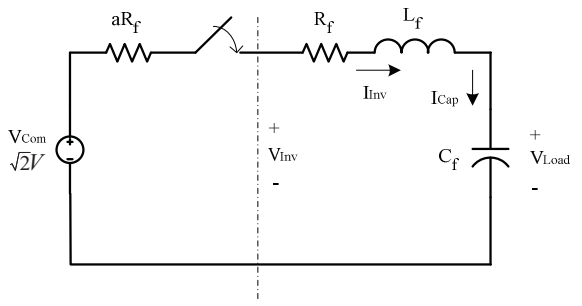


Fig. 4 Simplified equivalent circuit of PWM inverter system without load.

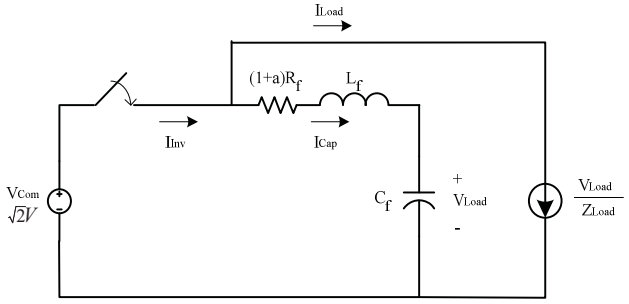


Fig. 5 Simplified equivalent circuit of PWM inverter system with full load.

The inverter current can be calculated by (7).

$$i_{INV} = \frac{\sqrt{2}\omega_f C_f V}{\sqrt{1-\xi_c^2}} e^{-\xi_c \omega_f t} \cdot \sin(\omega_f \sqrt{1-\xi_c^2}\, t) \,. \qquad (7)$$

The inverter current described by (7) has maximum value when time reaches to (8).

$$t_m = \frac{\cos^{-1}\xi_c}{\omega_f \sqrt{1-\xi_c^2}} \,. \qquad (8)$$

Thus maximum inverter current can be calculated by (9).

$$I_{INVMax} = \sqrt{2}\sqrt{\frac{C_f}{L_f}} \cdot V \cdot e^{-\cos^{-1}\xi_c / (\sqrt{1-\xi_c^2}/\xi_c)} \qquad (9)$$

Since $I_{INVMax} < \sqrt{2}I$ where $I = V/Z_{Load}$, the proportion between the filter inductance and the filter capacitance should be limited by (10).

$$\sqrt{\frac{L_f}{C_f}} > Z_{Load} \cdot e^{-\cos^{-1}\xi_c / (\sqrt{1-\xi_c^2}/\xi_c)} \approx Z_{Load} \cdot e^{-\xi_c} \,. \qquad (10)$$

B. Equivalent Circuit With Full Load

Although the output LC filters are a main cause to the inverter current stress in the transient state, load current also adds the current stress during the transient state. When the

load is inductive, the effect of the load current to the inverter transient current is not so significant since it increases smoothly after load terminal voltage is established. However when the load is purely resistive, the load current can not be neglected, since it increases sharply proportional to the established load voltage.

The equivalent circuit of the PWM inverter system with a full load can be described by Fig.5 since inverter output current I_{Inv} is a sum of the filter capacitor current I_{Cap} and the load current I_{Load}. Here, the oscillation damping voltage V_{Damp} and the disturbance rejection voltage $V_{Disturb}$ are assumed to be ideally controlled. In worst case, the reference load voltage with the magnitude of $V_{Load}^{*} = \sqrt{2}V$ is suddenly commanded to the PWM inverter system at time t=0. Worst case can also occurs when the load impedance is purely resistive $Z_{Load}=R_{Load}$.

When the output regulating voltage V_{Com} is exactly regulated to the reference load voltage V_{Load}^{*} by a normal feed forward controller, then the load voltage becomes like (11).

$$V_{Load} = \frac{\omega_f^2}{s^2 + 2\xi_c\omega_f s + \omega_f^2} V_{Load}^{*} = \frac{\omega_f^2 \sqrt{2}V}{s\left(s^2 + 2\xi_c\omega_f s + \omega_f^2\right)} \quad (11)$$

Thus the filter capacitor current I_{Cap} and the load current I_{Load} can be calculated by (12) and (13) respectively.

$$I_{Cap} = sC_f V_{Load} = \frac{\sqrt{2}C_f V\omega_f^2}{s^2 + 2\xi_c\omega_f s + \omega_f^2}, \quad (12)$$

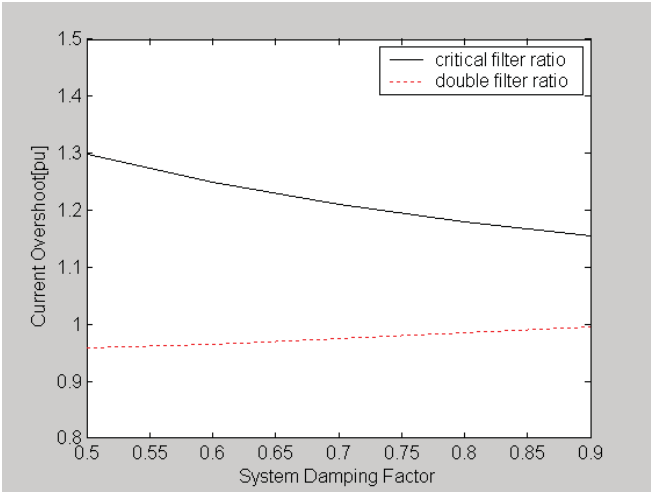


Fig. 6 Inverter Current Overshoot Depending On Filter Ratio.

$$I_{Load} = \frac{V_{Load}^{*}}{Z_{Load}} = \frac{\sqrt{2}V}{R_{Load}} \cdot \frac{\omega_f^2}{s\left(s^2 + 2\xi_c\omega_f s + \omega_f^2\right)}. \quad (13)$$

When the filter ratio is chosen as $\sqrt{L_f / C_f} = R_{Load} / 2\xi_c$ that is a critical value when $R_{Load} = (1+a)R_f$, the filter capacitor current can be described by (14).

$$I_{Cap} = \frac{\sqrt{2}V}{R_{Load}} \cdot \frac{2\xi_c\omega_f}{s^2 + 2\xi_c\omega_f s + \omega_f^2}. \quad (14)$$

Then the inverter output current $i_{Inv}(t)$ in time domain can be calculated by the sum of the filter capacitance current $i_{Cap}(t)$ and the load current $i_{Load}(t)$ as (15).

$$i_{Inv}(t) = i_{Cap} + i_{Load} = \frac{\sqrt{2}V}{R_{Load}} \cdot \left[1 + \frac{e^{-\xi_c\omega_f t}}{\sqrt{1-\xi_c^2}} \cdot \sin\left(\omega_f\sqrt{1-\xi_c^2}\cdot t - \cos^{-1}\xi_c\right)\right] \quad (15)$$

Since the inverter current reaches to a maximum value at $t_m = 2\cdot\cos^{-1}\xi_c / (\omega_f\sqrt{1-\xi_c^2})$, the maximum inverter current can be calculated by (16).

$$I_{InvMax} = \frac{\sqrt{2}V}{R_{Load}} \cdot \left(1 + e^{-\frac{\xi_c}{\sqrt{1-\xi_c^2}}\cos^{-1}\xi_c}\right). \quad (16)$$

When the filter ratio is set twice to the critical ratio as $\sqrt{L_f / C_f} = R_{Load} / \xi_c$, the maximum inverter current can be calculated by (17).

$$I_{InvMax} = \frac{\sqrt{2}V}{R_{Load}} \cdot \left(1 - \sqrt{1-\xi_c^2}\cdot e^{-\left(\frac{\pi - \cos^{-1}\sqrt{1-\xi_c^2}}{\sqrt{1-\xi_c^2}}\right)}\right). \quad (17)$$

Fig.6 shows the inverter current overshoot calculated by (16) and (17) depending on the filter ratio when the system damping factor ranges from 0.5 to 0.9. When the filter ratio is set to the critical value, the inverter current overshoot decreases according to the system damping factor while it is always higher than 1.15. When the filter ratio is set two times to the critical value, the inverter current overshoot is always less than 1.0.

Thus in pure resistive loads, the filter ratio may be set to $\sqrt{L_f / C_f} < R_{Load} / \xi_c$ to maintain the inverter output current under the rated peak value in the transient state. When the load is highly inductive, the filter ratio can be decreased to (10). The lower filter ratio is better since large filter inductors result to load current disturbance, cost and weight issues of the output filters, and voltage stress on the inverter.

Therefore, this paper proposes a filter design guide line in deciding the filter ratio as (18).

$$\frac{Z_{Load}}{\xi_c} \geq \sqrt{\frac{L_f}{C_f}} \geq \frac{Z_{Load}}{e^{\xi_c}}, \qquad (18)$$

where, upper bound is for purely resistive full load,
lower bound is for no load, and
middle region is for inductive loads or partial loads.

IV. Experimental Result

Fig.7 shows the experimental set up to verify the proposed design criterion on the output LC filter. The experiment is performed for a single phase inverter module. Experimental conditions are shown in Table I. A sinusoidal reference load voltage is applied when its magnitude is the maximum value of 120V. The inverter is composed of 4 IGBT switches with the switching frequency of 10 kHz. The sampling time of digital control system is 10 kHz, which is based on a TMS320VC33/150MHz processor.

TABLE I EXPERIMENTAL CONDITIONS

V_{CMAX}	120V
Z_{Load}	5Ω resistive
Fsw	10kHz
Fc	840Hz

Since the filter cutoff frequency is set to 840Hz as given by Table I, the control bandwidth of the proposed controller can be reached to 840Hz and the PWM inverter system can synthesize voltage harmonics up to the 13TH order. Further, the harmonic attenuation at the switching frequency is about -43dB so that only 0.7% of the voltage ripple due to the inverter switching remains in the output load voltage as a noise. Generally, the combinations of filter inductor and filter capacitor for a given filter cut off frequency are infinite. However, since the load is pure resistive, the combination of filter inductor and filter capacitor can be uniquely decided based on the proposed design criterion as Table II by the upper bound of (18).

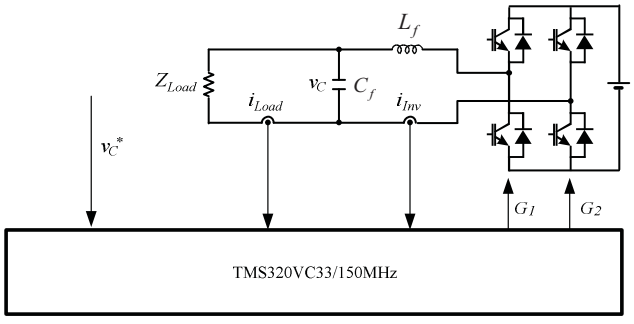
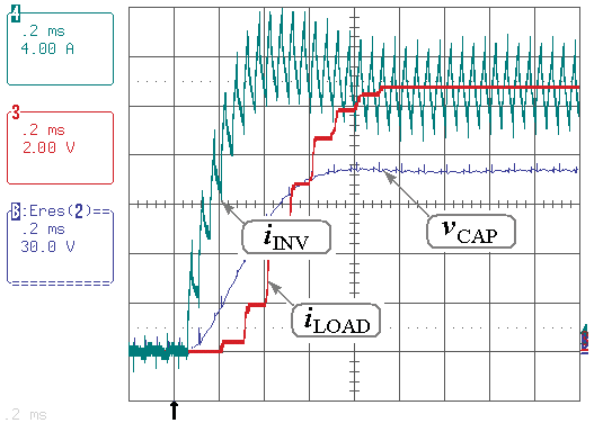


Fig. 7 Experimental set up.



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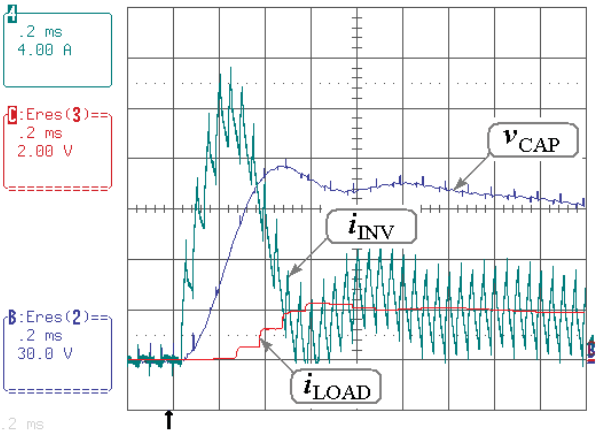

b)

Fig. 8 Experimental waveforms when the sampling time and the PWM switching frequency is 10kHz, system damping factor is 0.5, and the load is pure resistive (horizontal axis: 0.2ms/div, vertical axis: 4.00A/div or 30.0V/div); a) when $\sqrt{L_f / C_f} = Z_{Load}$, b) when $\sqrt{L_f / C_f} = Z_{Load} / 4$.

TABLE II. DESIGNED FILTER INDUCTOR AND CAPACITOR

fc	840Hz
L_f	900μH
C_f	40μF

Fig.8 shows the experimental waveforms of the transient response where system damping factor is set to 0.5 and the load is pure resistive. Fig.8a) is the waveforms when the combination of filter inductor and filter capacitor was designed $\sqrt{L_f / C_f} = Z_{Load}$ according to (18). While the load current settles into around 21.6 A, the inverter current overshoots around 24A in its center value, which means the inverter current goes over 1.1 times to the rated peak current. Considering normal safety factors on IGBT switches this over current is not matter.

Fig.8b) is the waveforms when the combination of filter inductor and filter capacitor was adjusted to $\sqrt{L_f / C_f} = Z_{Load} / 4$ by replacing the load resistor with 20Ω that is four times larger than that of Fig.8a). While the load current settles into around 4A, the inverter current overshoot reaches up to around 19A in its center value, which means the inverter current goes over 4.75 times to the rated peak current. This over current will conflict with typical safety factors on IGBT switches. The output load voltage v_{Cap} also shows some oscillatory behavior.

Fig.9 shows the experimental waveforms for the steady state response of the proposed inverter system with the same filters as in Fig.8. The peak value of the inverter ripple current in steady state goes around 1.2 times to the rated peak value in Fig.9a) where the combination of filter inductor and filter capacitor was designed $\sqrt{L_f / C_f} = Z_{Load}$. While it goes around 1.8 times to the rated peak value in Fig.9b) where the combination of filter inductor and filter capacitor was designed $\sqrt{L_f / C_f} = Z_{Load} / 4$. This may also conflict with the current specification on the inverter switches.

V. Conclusion

This paper has discussed on output filter design considering both the control dynamics and the inverter size of PWM inverter systems. While the cut off frequency of output LC filters limits theoretical control bandwidth, it attenuates the switching ripples that appear in the output voltages of PWM inverters. Although there are infinite combinations of filter inductor and filter capacitor for a given filter cutoff frequency, no analytical design method was presented before. This paper analyzed the relation among the output LC filter, PWM inverter, and controller in inverter systems to provide a design criterion for the output LC filters which does not give over current stress to the inverter switches nor degraded control performance to the PWM inverter system. Experimental results have verified that the proposed output LC filter ensures optimal inverter size and good control dynamics of PWM inverter systems.

Acknowledgment

This work was supported partly by the fund of the Korea Research Foundation.

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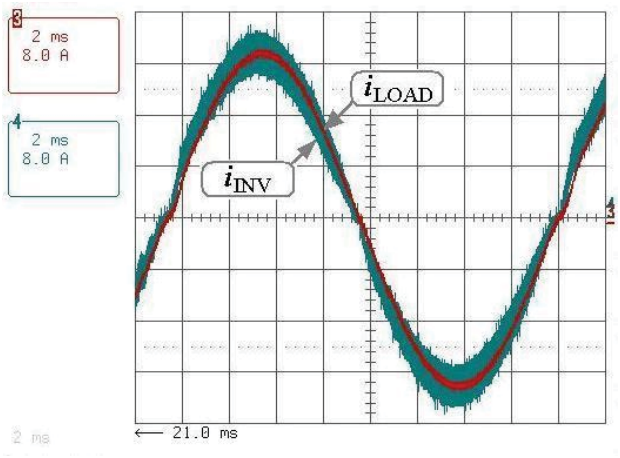

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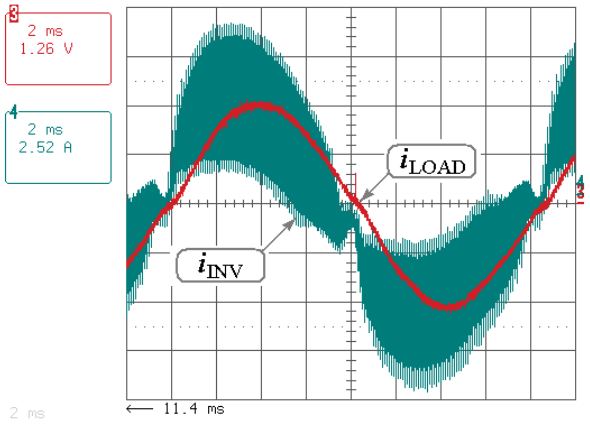

b)

Fig. 9 Experimental waveforms when the sampling time and the PWM switching frequency is 10kHz, system damping factor is 0.5, and the load is pure resistive (horizontal axis: 0.2ms/div, vertical axis: 4.00A/div or 30.0V/div); a) when $\sqrt{L_f / C_f} = Z_{Load}$, b) when $\sqrt{L_f / C_f} = Z_{Load} / 4$.

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