DC-link Voltage Stabilization for Reduced DC-link Capacitor Inverter

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***Abstract* -- A PMW inverter with reduced dc-link capacitor has a problem that the dc-link voltage is less stable compared to the conventional inverter because of the lack of energy storage capability. The proposed dc-link voltage stabilization algorithm using active damping gives a solution to this problem. To achieve load/source independent stabilization, the source state estimator which estimates both source voltage and current is also proposed. The proposed methods are evaluated by experimental results. While the inverter with a small DC link capacitor tripped due to dc-link overvoltage fault at step load change, the fluctuation of dc-link voltage of the inverter is suppressed under the tolerance range with the proposed method at the same step load change.**

***Index Terms*-- Pulse width modulated inverters, dc-link capacitor, DC-link voltage stabilization, Active damping**

I. INTRODUCTION

PWM inverter for ac drive is a power converter to synthesize ac voltage from a dc-link voltage. The dc-link capacitors in the PWM inverter act as an energy buffer to stabilize the dc-link voltage and keep it almost constant. Thus, electrolytic capacitors with large capacitance per unit volume have been commonly used as dc-link capacitors. However, the electrolytic capacitors in the dc-link are bulky and make the inverter less reliable because of their short life time expectancy. Moreover, the large dc-link capacitance causes the large total harmonic distortion (THD) of the input source current when used with 3-phase passive rectifier such as 3-phase diode rectifier. As a result, there have been significant efforts to replace the electrolytic capacitors with a small film capacitor [1], [2].

However, the dc-link voltage of the inverter may be unstable resulting over-voltage or under-voltage faults due to reduced dc-link capacitance if the source inductance is large relative to the dc-link capacitance. This issue becomes significantly serious in the case that the inverter is supplying large power to Constant Power Loads (CPL) because the constant power loads have negative dynamic impedance characteristic [3]-[5]. Due to this negative impedance characteristic, if the dc-link voltage is getting larger, the dc-link current is getting smaller so as to maintain constant power to the load. This reaction can result in over voltage or under voltage at the dc-link.

The problem due to the negative impedance characteristic can be prevented by designing the input filter whose parameters satisfy the stability criterion [3]. If the filter parameters are fixed, passive damping resistors can be added in order to change the system impedance. However, the passive damping resistors always cause additional losses in the system.

In [3]-[5], the fluctuating dc-link voltage is actively stabilized by changing the dynamic impedance seen from the dc-link to be positive. Changing impedance can be achieved by modifying the current command because the output power is directly related to the output current [4]. If the dc-link voltage fluctuation frequency is over the current control bandwidth, voltage commands are modified instead of current command [3], [5]. These methods, however, assume that the input source voltage to be constant dc to employ linearized control law. This assumption makes the dynamic impedance of the inverter be dc-link voltage dependent because the changed impedance is directly related to the dc-link voltage. Moreover, the method in [5] requires load impedance in the control law.

Also, the rapid load changes can result in the dc-link over voltage or under voltage [6]. For instance, if the output power increase stepwise there will be a huge voltage dip at the dc-link because the energy stored in the capacitor is not enough to maintain the dc-link voltage. To prevent this transient dc-link voltage fluctuation and regulate the dc-link voltage variation within a tolerable range, the inverter response (or control bandwidth) should be reduced down sufficiently. As a result, the overall performance would be degraded because of the reduced control bandwidth.

In this paper, a novel dc-link voltage stabilizing method is proposed. The stabilization is basically based on the active damping which changes the dynamic impedance of the system by directly modifying the inverter output voltage. In order to eliminate the effect of (grid) source voltage variation, both the estimated source state (source voltage) and dc-link voltage are used in the control law. A closed-loop estimator to obtain the predicted source states (source voltage and source current) is proposed. Furthermore, to suppress the transient dc-link voltage fluctuation within an tolerable range, a simple dc-link voltage regulation method is also proposed. To control the dc-link voltage variation, inverter output voltage is modified using both the predicted dc-link voltage and the source current from the estimator. With the proposed methods, the inverter with reduced dc-link capacitor can be kept operating

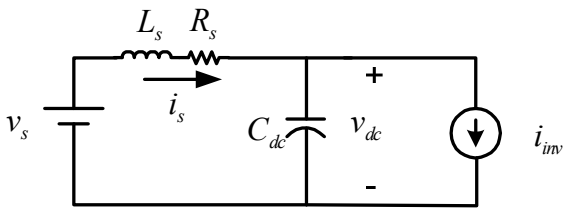


Fig. 1. Source/Inverter/Load equivalent model

without any fault from both the instability due to the constant power load and dc-link voltage fluctuation due to the rapid load change.

II. Instability Due To Reduced Dc-link Capacitor

Fig. 1 is the system model including the source, inverter, and load neglecting the PWM of the inverter. The inverter and load are modeled as a current source(i_{inv}). L_s and R_s are the equivalent source impedance, and C_{dc} is the dc-link capacitance. The dynamic equations of the system shown in Fig 1 are described by

$$L_s \frac{di_s}{dt} = v_s - R_s i_s - v_{dc} \quad (1)$$

$$C_{dc} \frac{dv_{dc}}{dt} = i_s - i_{inv} \quad (2)$$

If the load power is constant as P_L, the inverter current, i_{inv}, can be expressed as

$$i_{inv} = P_L / v_{dc} = \frac{P_L}{v_{dc0} + \tilde{v}_{dc}} \quad (3)$$

where v_{dc0} is a mean value of the dc-link voltage, and $\tilde{v}_{dc}$ is a dc-link voltage variation. If $\tilde{v}_{dc}$ is relatively small to its mean value, the inverter current can be linearlized as (4).

$$i_{inv} = \frac{P_L}{v_{dc0} + \tilde{v}_{dc}} \cong \frac{P_L}{v_{dc0}} - \frac{P_L}{{v_{dc0}}^2} \tilde{v}_{dc} \quad . \quad (4)$$

From (4), it can be shown that the constant power load acts as negative impedance against dc-link voltage variation. With the linearized inverter current, the dynamic equations in (1) and (2) have following characteristic equation.

$$s^2 + (\frac{R_s}{L_s} - \frac{P_L}{C_{dc}{v_{dc0}}^2})s + (\frac{{v_{dc0}}^2 - R_s P_L}{L_s C_{dc}{v_{dc0}}^2}) = 0 \, . \quad (5)$$

From (5), the stability criterion for the dc-link capacitor can be obtained as

$$C_{dc} > \frac{L_s P_L}{R_s {v_{dc0}}^2} \, . \quad (6)$$

Thus, if the capacitance of the inverter does not satisfy the criterion in (6), the system states including the dc-link voltage are unstable or oscillating. As a result, the semiconductor switches such as IGBTs can be destroyed from over-voltage break-down.

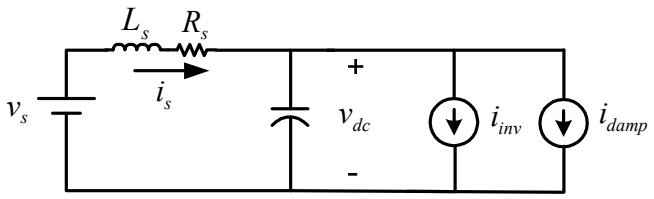
III. Proposed Stabilization Method

The dc-link instability problem can be solved by manipulating the torque-producing current command [4]. However, if the oscillation frequency which is related to the system parameters is too high for the bandwidth of the current regulator to generate additional manipulating current, the instability does not disappear even with the stabilizing controller. Therefore, manipulating directly voltage command instead of current command is suitable for suppressing the high frequency oscillation.

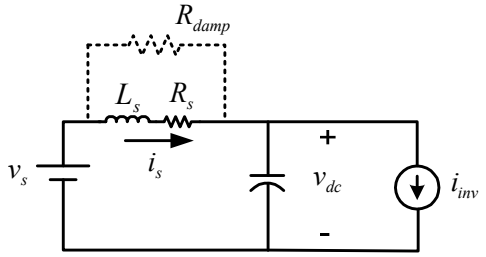
A. DC-link voltage stabilization method for constant power load

From the system model in Fig. 1, a virtual damping resistor can be added between the source voltage and the dc-link capacitor in order to regulate the dc-link voltage to the source voltage as shown in Fig. 2. The active damping is achieved by injecting additional inverter current (i_{damp}) which is proportional to the difference between the dc-link voltage and the estimated source voltage.

$$i_{damp} = \frac{(v_{dc} - \hat{v}_s)}{R_{damp}} \quad (7)$$



(a)



(b)

Fig. 2. (a) Damping current(i_{damp}) injection and (b) its effect to the dc-link capacitor Source/Inverter/Load equivalent model

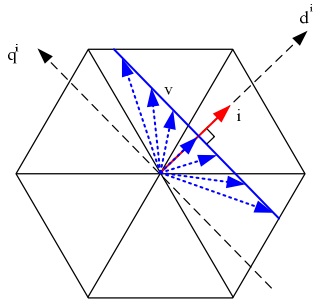


Fig. 3. Solution vectors that produce the damping current (i_{damp}) on the voltage vector space.

where $\hat{v}_s$ is the estimated source voltage. As the R_{damp} decrease, the dc-link is tightly regulated to the source voltage.

Injection of the additional damping current (i_{damp}) to the load can be achieved by adding additional voltage vector, $\vec{v}_{damp}$, to the original voltage command vector from the current regulator for the motor control. The damping voltage vector, $\vec{v}_{damp}$ that produces the damping current (i_{damp}) can be obtained from the following equations.

$$i_{damp} = \frac{3}{2}\frac{\vec{v}_{damp}\cdot\vec{i}_{dq}^{\,\omega}}{v_{dc}} \tag{8}$$

where the $\vec{i}_{dq}^{\,\omega}$ is the load current vector in the d-q rotating frame.

There are infinite solutions of $\vec{v}_{damp}$ satisfying the equation (8) because the equation is a 2-D vector equation, and the solutions lie on the line which is vertical to the current vector as shown in Fig. 3. The best solution is the vector that has minimum magnitude because $\vec{v}_{damp}$ is basically a voltage error to the current regulator. As a result, the additional damping voltage, $\vec{v}_{damp}$ on the axis where the load current vector lies is the optimal one. Because the solution vector lies on the load current vector, it is convenient to calculate the solution in the load current reference frame where all load currents lie on the d-axis of the frame. In the load current reference frame, the vector equation (8) can be transformed to the scalar equation as (9).

$$v_{damp}^{i} = \frac{2}{3}\frac{v_{dc}i_{damp}}{i_{load}} \tag{9}$$

where i_{load} is the magnitude of the load current, and the superscript, i, means the load current reference frame.

After calculating the additional voltage vector to inject from (9), the voltage vector is added to the original voltage command from the current regulator. The block diagram of the whole controller is shown in Fig. 4.

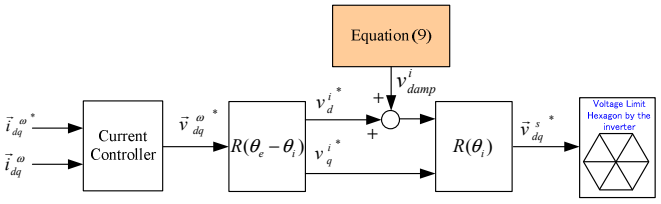


Fig. 4. Proposed dc-link stabilization controller and the frame transformation to the load current reference frame

B. *Source state estimator*

To achieve active damping effect as shown in Fig. 2(b), the source voltage that is not measurable is needed. To estimate the source voltage, the source state estimator is proposed. In the model depicted in Fig. 1, the states (voltage and current) of the source side can be estimated because the inverter current is a known control variable and the system is completely observable. Also, the averaged inverter current over one PWM period (i_{inv}) can be calculated from the inverter voltage output ($\vec{v}_{dq}^{\,\omega}$) and the load(machine) current($\vec{i}_{dq}^{\,\omega}$) as follows.

$$i_{inv} = \frac{3}{2}\frac{\vec{v}_{dq}^{\,\omega}\cdot\vec{i}_{dq}^{\,\omega}}{v_{dc}} \tag{10}$$

Neglecting the source resistance for simplicity, the state space system equation can be deduced as (11).

$$\begin{bmatrix}\dot{v}_{dc}\\ \dot{v}_s\\ \dot{i}_s\end{bmatrix} = \begin{bmatrix}0 & 0 & \frac{1}{C_{dc}}\\ 0 & 0 & 0\\ -\frac{1}{L_f} & \frac{1}{L_f} & 0\end{bmatrix}\begin{bmatrix}v_{dc}\\ v_s\\ i_s\end{bmatrix} + \begin{bmatrix}-\frac{1}{C_{dc}}\\ 0\\ 0\end{bmatrix} i_{inv} \tag{11}$$

From the system model and the system input(i_{inv}), it is possible to build an estimator where L is a gain matrix of the estimator.

$$\begin{bmatrix}\dot{\hat{v}}_{dc}\\ \dot{\hat{v}}_s\\ \dot{\hat{i}}_s\end{bmatrix} = \begin{bmatrix}0 & 0 & \frac{1}{C_{dc}}\\ 0 & 0 & 0\\ -\frac{1}{L_s} & \frac{1}{L_s} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_{dc}\\ \hat{v}_s\\ \hat{i}_s\end{bmatrix} + \begin{bmatrix}-\frac{1}{C_{dc}}\\ 0\\ 0\end{bmatrix} i_{inv} + L\left[v_{dc} - \begin{bmatrix}1 & 0 & 0\end{bmatrix}\begin{bmatrix}\hat{v}_{dc}\\ \hat{v}_s\\ \hat{i}_s\end{bmatrix}\right] \tag{12}$$

From the estimator in (12), the source voltage, v_s, and current, i_s, can be estimated without any additional measurement but the dc-link voltage. The discrete time prediction estimator of the continuous time estimator is expressed as

$$\begin{bmatrix}\hat{v}_{dc}[k+1]\\ \hat{v}_s[k+1]\\ \hat{i}_s[k+1]\end{bmatrix}=\Phi\begin{bmatrix}\hat{v}_{dc}[k]\\ \hat{v}_s[k]\\ \hat{i}_s[k]\end{bmatrix}+\Gamma i_{inv}[k]+\begin{bmatrix}L_1\\ L_2\\ L_3\end{bmatrix}[v_{dc}[k]-\hat{v}_{dc}[k]] \quad (13)$$

where

$$\Phi=\begin{bmatrix}\cos\frac{T}{\sqrt{L_sC_{dc}}} & 1-\cos\frac{T}{\sqrt{L_sC_{dc}}} & \sqrt{\frac{L_s}{C_{dc}}}\sin\frac{T}{\sqrt{L_sC_{dc}}}\\ 0 & 1 & 0\\ -\sqrt{\frac{C_{dc}}{L_s}}\sin\frac{T}{\sqrt{L_sC_{dc}}} & \sqrt{\frac{C_{dc}}{L_s}}\sin\frac{T}{\sqrt{L_sC_{dc}}} & \cos\frac{T}{\sqrt{L_sC_{dc}}}\end{bmatrix}$$

$$\Gamma=\begin{bmatrix}-\sqrt{\frac{L_f}{C_{dc}}}\sin\frac{T}{\sqrt{L_sC_{dc}}}\\ 0\\ 1-\cos\frac{T}{\sqrt{L_sC_{dc}}}\end{bmatrix}$$

From the prediction source state estimator, the source voltage and the source current can be obtained without measurement.

C. DC-link voltage stabilization method for rapid load change

From the source state estimator, the source current, i_s, which can not vary rapidly during one PWM period because of the source inductance, can be estimated. And, the inverter output current, i_{inv}, during the next PWM period is a control variable. Hence, it is possible to predict the dc-link capacitor current using the estimated source current and the inverter current during the next PWM period. With this predicted source current and the inverter current, It is also possible to predict the dc-link voltage variation if the dc-link capacitance is known. The dc-link voltage variation during the next PWM period can be described as follow.

$$\Delta v_{dc}[k+1]=\frac{T}{\hat{C}_{dc}}(\hat{i}_s[k+1]-i_{inv}[k+1]) \quad (14)$$

where Δv_{dc} is the dc-link voltage variation after one control period, T, and $\hat{C}_{dc}$ is the estimated dc-link capacitance.

Because the film capacitor has quite tight tolerance of capacitance less than 20% for its life time, the dc-link voltage variation can be predicted quite accurately. In other words, it is possible to regulate the dc-link voltage within a tolerable range by restricting i_{inv} if the dc-link voltage could be out of the range during the transient such as the rapid load change. Because the i_{inv} is an inner product of output voltage vector and load current vector, the desired dc-link voltage which makes the dc-link voltage bounded in a desired range is represented as a band-shaped area of tolerable output voltage which is vertical to the load current vector on the voltage vector space as shown in the Fig. 5(a). Therefore, the final voltage command should be on the band to avoid the dc-link over/under voltage. Thus, if the calculated voltage command is out of the band, the voltage command should be moved into the band. For example, if the voltage command is out of the band, it is projected on the boundary of the band as shown in Fig. 5(b) to minimize the voltage modification. If the upper and lower limit of the dc-link voltage is defined as V_{dc_max} and V_{dc_min} respectively, the voltage command limits in the d-axis of the load current reference frame can be deduced as

$$v_d^{i\,*}[k]i_d^i[k]>\frac{2}{3}\hat{v}_{dc}[k+1]\{\hat{i}_s[k+1]-\frac{\hat{C}_{dc}}{T}(V_{dc\_max}-\hat{v}_{dc}[k+1])\} \quad (15)$$

$$v_d^{i\,*}[k]i_d^i[k]<\frac{2}{3}\hat{v}_{dc}[k+1]\{\hat{i}_s[k+1]-\frac{\hat{C}_{dc}}{T}(V_{dc\_min}-\hat{v}_{dc}[k+1])\} \quad (16)$$

Thus, the dc-link voltage can not be out of the desired range after the d-axis voltage command is limited by (15) and (16) even with rapid load change.

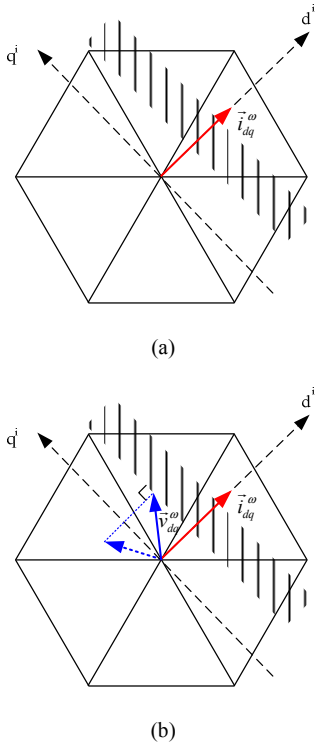


Fig. 5. (a) Voltage command band to avoid dc-link over/under voltage (b) Voltage command projection to the boundary of the band

IV. Experimental Results

Some experiments were carried out to verify the proposed methods. The motor used in the experiment is a 2kW permanent magnet synchronous motor. The dc-link capacitance is 9μF and the per-phase inductance of the source is 1.5mH. 3-phase 110Vrms voltage source and a diode rectifier were used as a dc voltage source to dc-link.

Fig. 6 shows the stabilization of the proposed method before and after applying the proposed stabilization methods. Before applying the method, as shown in Fig. 6(a), both the dc-link voltage and source current are unstable and fluctuating. After applying the proposed method in III.A, both the source current and the dc-link voltage are well stabilized as shown in Fig. 6(b). Fig. 7(a) shows the dc-link voltage spike over 100V at the step load change, and the spike results in over voltage trip of the inverter. Fig. 7(b) depicts the result with the same load change using the proposed algorithm in III.C. Because the maximum voltage limit was set to 200V, the dc-link voltage was limited by 200V as shown in Fig. 7(b).

V. Conclusion

In this paper, new dc-link voltage stabilization methods for the PWM inverter with the reduced dc-link capacitor were proposed. The proposed stabilization algorithm is independent from the source/load variation because it has been designed based on the estimated source voltage. By directly manipulating the output voltage command, the voltage oscillation whose frequency is over the bandwidth of the current regulator can be suppressed effectively. Moreover, the proposed method does not degrade the current controller dynamics during the normal operation because it automatically works only while the dc-link voltage is predicted to be out of tolerable range. The performance and effectiveness of the proposed methods was evaluated by several experimental results.

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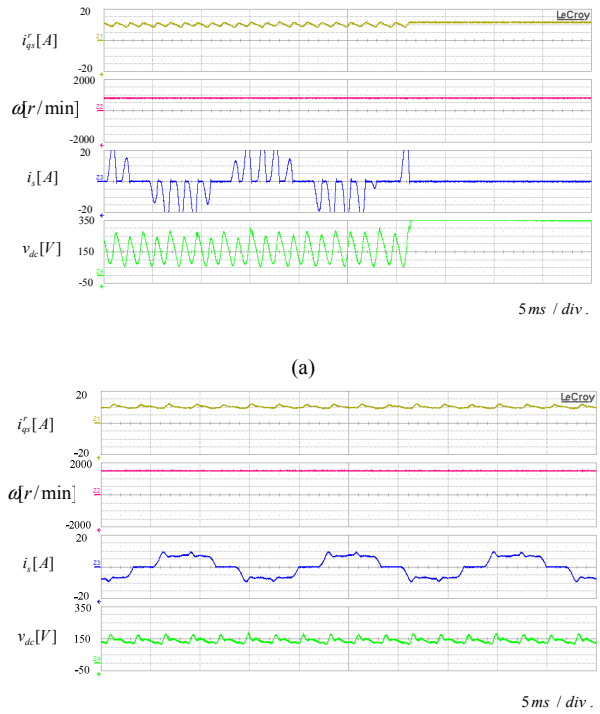
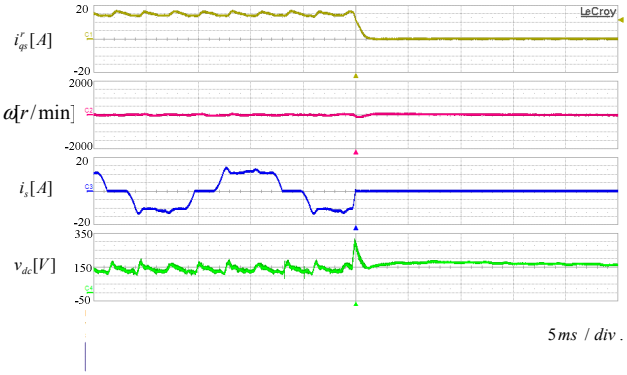


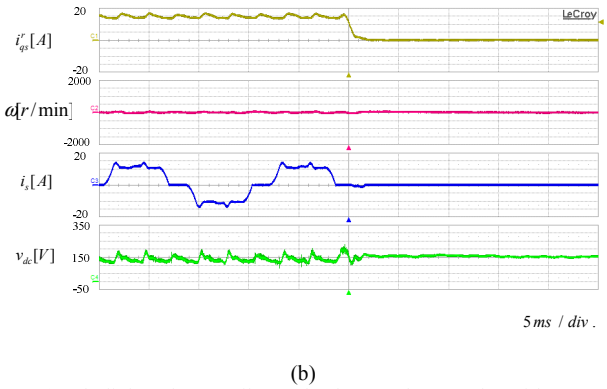
(a)

(b)

Fig. 6. Constant power output waveforms : (a) without stabilization method; (b) with proposed method.



(a)



(b)

Fig. 7. (a) dc-link voltage spike at load step change; (b) with proposed method.