Design of Speed and Current Regulator Minimizing Time Delay from Digital Control

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1. Introduction

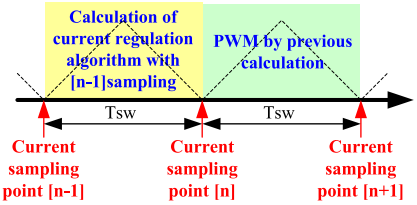
The Linear permanent magnet Synchronous Machine (LSM) is widely used for SMD mounting machine and semiconductor manufacturing devices which require the high speed linear motion. To increase the productivity of the manufacturing process in these applications, the high bandwidth of speed and current regulation should be achieved. In the cascade control system, the bandwidth of the speed control is dependent on that of the current regulator. Also, the bandwidth of the current regulator is restricted by the switching frequency of the switching devices. In the case of above the several hundreds watts of servo drive system, its switching frequency is limited up to around 10[kHz] due to avoiding the excessive switching losses. Because of the limited switching frequency, the bandwidth of the current regulation can not be extended and the restricted bandwidth of the current regulator is directly related to the current regulation response and also to the speed control bandwidth. There have been several preferred approaches that enhance the current regulation bandwidth under limited switching frequency. In [1], the internal model controller (IMC) which has low complexity is proposed. The dynamic decoupling current controller and the complex vector current regulator are robust to the variety of the inductance [2],[3]. And the current prediction regulator and deadbeat current regulator can reduce the torque ripples [4]. These conventional methods, however, still have a digital problem which is inherent problem where the Digital Signal Processor (DSP) or microcontroller is utilized.

Another limiting factor in the current regulation is time delay due to digital control. The delay in PWM inverter driven servo system consists of mainly two factors, execution time of the algorithm and PWM itself. Many researchers have tried to reduce the digital delay to enhance the performance of current regulator [5], [6]. In [6], the current regulator has been implemented with hardware. This method, however, is quite time-consuming and has less flexibility.

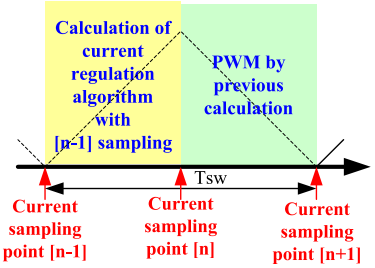
This paper represents a novel design strategy, which minimizes the digital execution time of the current regulator, and it results in faster response and more precise current regulation. Also, the proposed strategy can increase the bandwidth of speed control appreciably.

2. Analysis of Conventional Current Regulation

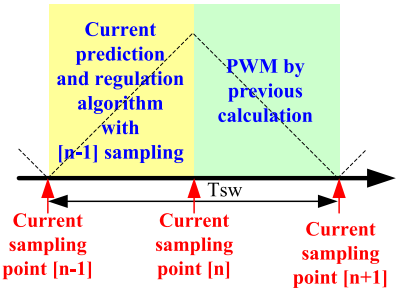
In this section, the timing diagrams of PWM inverter driving a servo system are analyzed to clarify the time delays of the conventional design strategy of the current regulator. Fig.1 shows the timing diagram of the conventional current regulation schemes of PWM inverter in the discrete or digital domain with a triangular PWM carrier.



(a) Current sampling at peak or valley of carrier and delay.



(b) Current sampling at peak and valley of carrier and delay.



(c) Current sampling at peak and valley of carrier, current prediction and delay.

Figure 1: Current sampling and delays.

To reduce the current ripple, it is prerequisite to sample the average value of the current in a sampling period [7]-[9]. If the current is sampled at peak or valley of PWM carrier, the average value can be obtained under the condition of symmetry PWM gating signals. Also, this kind of sampling increases the robustness of the current measurement to the switching noises on the feedback current.

If the current sampling executes at peak or valley of the carrier, that is once in a switching period, the total delay which is the sum of the algorithm execution time and PWM delay is 1.5 times of switching period, T_{sw}. In Fig.1 (a), the calculation of algorithms, which are based on [n-1] current sampling, spends the one switching time. And the voltage reference, which is output of the current regulator, is updated at every switching period and there is

a half of switching period time delay on the average sense. Therefore, the total delay of the current regulation which is based on the [n-1] current sampling is 1.5 times of switching period.

If the current sampling executes at peak and valley of the carrier, two times in a switching period, the delay would be reduced to 0.75 times of switching period, and it is a half of the previous case. In Fig.1 (b), the execution time is 0.5 times of switching period and the voltage references update spends 0.25 times of the switching period on the average.

Moreover, if the prediction of the current based on the sampled current is appended to the latter case, the execution time can be saved and the delay may be reduced up to the 0.25 times of switching period. In Fig.1 (c), the total delay is only related to the voltage reference update. In this case, however, the accuracy of the parameter should be guaranteed for the exact current prediction. Otherwise, the response of the current regulator may reveal unacceptable ripples.

3. Proposed Current Regulation Strategy

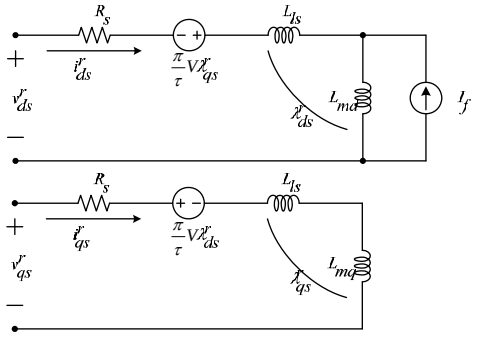


Figure 2 : Equivalent circuit of LSM.

Fig. 2 shows the equivalent circuit of the LSM. The d, q-axis stator voltage of LSM in synchronous rotating frame are written as

$$v^r_{dqs} = R_s\, i^r_{dqs} + \frac{d\,\lambda^r_{dqs}}{d\,t} - j\omega_r\,\lambda^r_{dqs} \qquad (1)$$

where $f^r_{dqs} = f^r_{ds} + j\, f^r_{qs}$, $\omega_r = \frac{\pi}{\tau}$ and τ: pole-pitch.

The flux linkage induced by the permanent magnet and stator currents are expressed as

$$\begin{bmatrix}\lambda^r_{ds}\\ \lambda^r_{qs}\end{bmatrix} = \begin{bmatrix}L_{ls}+L_{md} & 0\\ 0 & L_{ls}+L_{mq}\end{bmatrix}\begin{bmatrix}i^r_{ds}\\ i^r_{qs}\end{bmatrix} + \begin{bmatrix}L_m I_f\\ 0\end{bmatrix} \qquad (2)$$

From the equation (1) and (2), d, q-axis voltage equation can be rewritten as follows

$$v^r_{dqs} = R_s\, i^r_{dqs} + L_s\frac{d\, i^r_{dqs}}{dt} - j\omega_r\lambda^r_{dqs} \qquad (3)$$

where synchronous inductance, $L_s = L_{ls} + L_{md} = L_{ls} + L_{mq}$, and equivalent excitation current from permanent magnet , I_f , is constant.

In (3), the last term of the right side which is defined as the back-EMF can be cancelled by the cross coupling decoupling strategy when the inductance is known exactly. If the decoupling is done perfectly, LSM can be regarded as an R-L load.

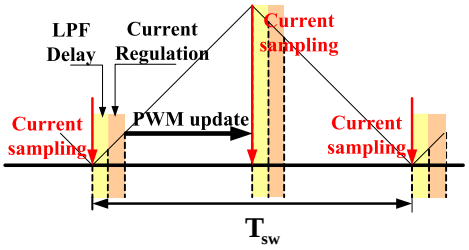


Figure 3 : The proposed current control strategy.

Fig.3 shows the timing diagram of the proposed strategy which reduces the digital execution time and PWM delay as small as possible. In this point of view, the proposed current regulator can be approximated closely to their analog counterpart. The current sampling point locates at peak and valley of the carrier. An analog Low Pass Filter (LPF) is essential to eliminate the switching noises on the sampled feedback current, and the delay time due to the filter cannot be reduced below a certain value. The execution time for current regulation algorithm is the calculation time to generate the voltage references from the synchronous frame Proportional Integral (PI) current regulator. In Fig.3, the proposed current regulator reduces the total digital execution time to a fraction of the current sampling period.

It seems that the proposed current regulator doesn't utilize the DC-link voltage maximally because of the analog filter delay and the algorithm execution delay in every rising/falling carrier. The servo motor driven by PWM inverter, however, has small back-EMF especially at low speed. Hence, at the low speed operation the voltage references locate near the center of the carrier, and the execution time delay doesn't influence seriously on current regulation performance in the sense of limited output voltage.

The voltage references are updated immediately after the current regulation. The total delay time of the proposed strategy is $0.25T_{sw}$ which represents the sum of the analog filter delay, digital execution time and PWM delay. It is the minimum delay time in the PWM inverter can achieve, because it come from the PWM itself. The digital delay of the proposed strategy is equal to the conventional current regulator using the prediction method mentioned previously. The proposed strategy, however, does not rely on the prediction, and it is robust to the parameter and reference variations.

If the execution time or analog filter delay can be reduced much more, the proposed current regulation strategy works similar to its continuous case. The gain of PI regulator can be set from the following equation (4)~(6). Suppose that the current regulation is well done when the current reference is i^{r*}_{dqs} and at the next instant, the current error, Δi^r_{dqs} is generated by the change of the current reference, the equation (4) should be satisfied for the current regulation.

$$K_P\,\Delta i^r_{dqs} + K_I\int \Delta i^r_{dqs}\,dt = R_s\left(i^r_{dqs} + \Delta i^r_{dqs}\right) + L_s\frac{\Delta i^r_{dqs}}{\Delta t} \qquad (4)$$

where

$K_P = \hat{L}_s \omega_{cc}$: Proportional gain of current regulator.

$K_I = \hat{R}_s \omega_{cc}$: Integral gain of current regulator.

$\hat{L}_s$: Estimated stator inductance.

$\hat{R}_s$: Estimated stator resistance.

ω_{cc} : Bandwidth of current regulator.

If the equation (4) is satisfied, the current regulator has similar dynamics with deadbeat regulator in which the current regulation is done at next sampling instant. The proposed method, however, has PI regulator which is more robust to the parameter variation than the deadbeat regulator is.

In the transient, the proportional gain at the left term of (4) which is output of the synchronous frame PI current regulator is dominant. And at the right side term which is the electrical model of LSM, the voltage drop across the resistance can be ignored. Hence, (5) can be obtained.

$$K_P \Delta i_{dqs}^r + K_I \int \Delta i_{dqs}^r \, dt \cong K_P \Delta i_{dqs}^r$$
$$L_s \frac{\Delta i_{dqs}^r}{\Delta t} + R_s \left(i_{dqs}^r + \Delta i_{dqs}^r \right) \cong L_s \frac{\Delta i_{dqs}^r}{\Delta t} \quad (5)$$

From (4) and (5), (6) can be acquired.

$$\hat{L}_s \omega_{cc} \Delta i_{dqs}^r = L_s \frac{\Delta i_{dqs}^r}{\Delta t} \quad (6)$$
$$\omega_{cc} = \frac{L_s}{\hat{L}_s} \frac{1}{\Delta t}$$

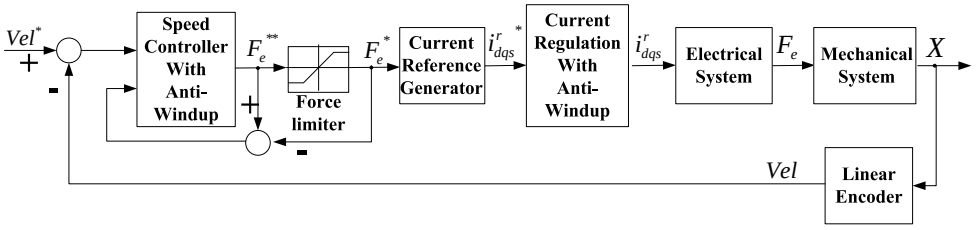
4. Speed Control with High-Bandwidth Current Regulator

In this section, the speed control method using the proposed current regulation for LSM is presented.

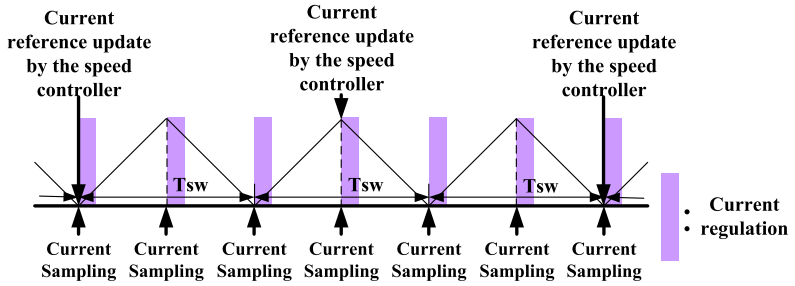
Fig.4 shows the speed control block diagram and timing diagram of LSM. In Fig.4 (a), the speed controller is PI controller which has been the most widely used in the real field. The velocity is calculated by using the M/T method or differentiation of the position for the evaluation of the performance of the current regulator clearly. In Fig.4 (b), the current reference, which is the output of the speed controller, is synchronized with current regulation.

Every 3 times of the current regulation, the current reference is updated by the speed controller. For target machine, the current settled down within 3 steps even though the current reference is changed from 0 to the rated value.

The transfer function of the speed control can be derived when the current regulation loop is considered as 1st order LPF $\left(\frac{i_{dqs}^r}{i_{dqs}^{r*}} = \frac{\omega_{cc}}{s + \omega_{cc}} \right)$.



(a) Speed control block diagram of LSM.



(b) Speed control timing diagram of LSM.

Figure 4 : Speed control block diagram and timing diagram of LSM.

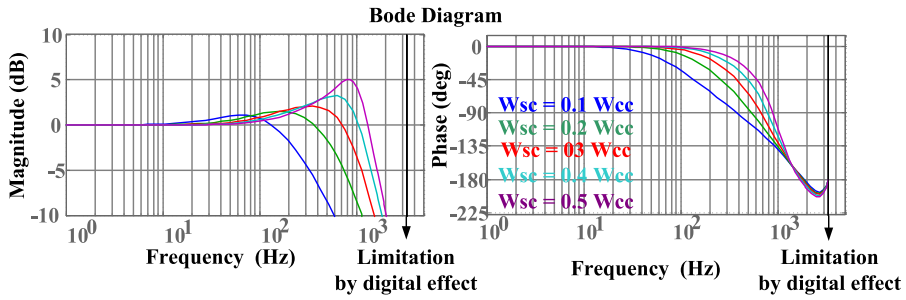


Figure 5 : Bode plot of speed control.

$$\frac{Vel}{Vel^*} = \frac{K_{PV}\,\omega_{cc}\,s + K_{IV}\,\omega_{cc}}{M\,s^3 + M\,\omega_{cc}\,s^2 + K_{PV}\,s + K_{IV}\,\omega_{cc}} \quad (7)$$

where

$K_{PV} = k_{sp1}\hat{M}\,\omega_{sc}$: proportional gain of speed controller

$K_{IV} = k_{sp2}\,K_{PV}\,\omega_{sc}$: integral gain of speed controller

ω_{sc} : bandwidth of speed controller

M : mover mass of LSM

$\hat{M}$: estimated mover mass of LSM

When the current regulation is fast enough in cascade speed control system, the transfer function for speed control can be expressed as following equation.

$$\frac{Vel}{Vel^*} = \frac{K_{PV}\,s + K_{IV}}{M\,s^2 + K_{PV}\,s + K_{IV}} \quad (8)$$

From (8), the specific gain k_{sp1} and k_{sp2} are related on the system damping.

$$\varsigma = \frac{1}{2}\sqrt{\frac{\hat{M}}{M}\frac{k_{sp1}}{k_{sp2}}} \quad (9)$$

where ς is system damping

Fig. 5 shows the Bode plot which demonstrates the interaction between the bandwidth of the current regulation and the bandwidth of speed control when the sampling rate of the speed is one third of that of current.

As shown in the Fig.5, the magnitude and the phase show reasonable performance when the bandwidth of the speed control is 0.1~0.2 times of that of the current regulator.

5. Experimental Results

In conventional servo system, the current reference is updated in sampling rated of the speed control loop which has lower sampling rate compared to the sampling rate of current loop. But in this study, to show the performance of the current regulator clearly, analog current reference is given to the regulator. Also, the Bode plot is used for evaluating the performance of the current regulator.

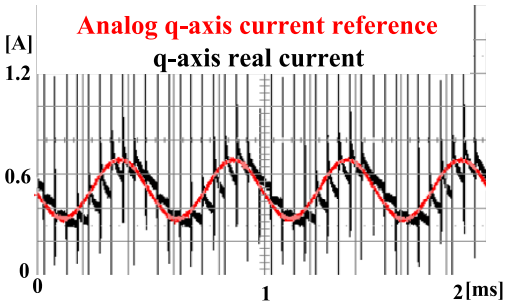
Generally, the current regulation loop is considered as the 1st LPF, therefore, the bandwidth of the regulator is defined as the frequency where 3[dB] attenuation or 45[deg] phase delay of the actual current compared to its reference.

The machine parameters under the test are shown in Table 1.

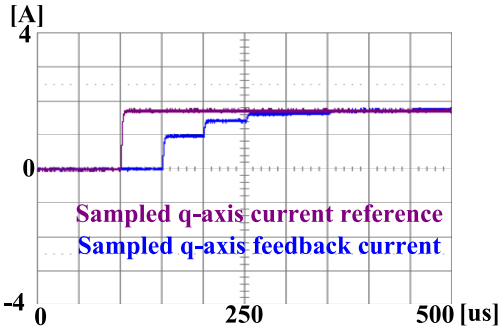
Fig.6 depicts the performance of the proposed current regulation, when the current reference is 2[kHz] sine

TABLE I. LSM Parameters

Quantity	Value [Unit]
rated force	$73[N]$
rated current	$1.2[A_{rms}]$
rated speed	$1.5[m/s]$
max. force	$220[N]$
max. current	$3.5[A_{rms}]$
stator resistance / phase	$12[\Omega]$
stator inductance / phase	$8.46[mH]$
Pole pitch	$22.5[mm]$



(a) 2[kHz] sinusoidal input.



(b) Rated current step input.

Figure 6 : Experimental result of the proposed current regulator.

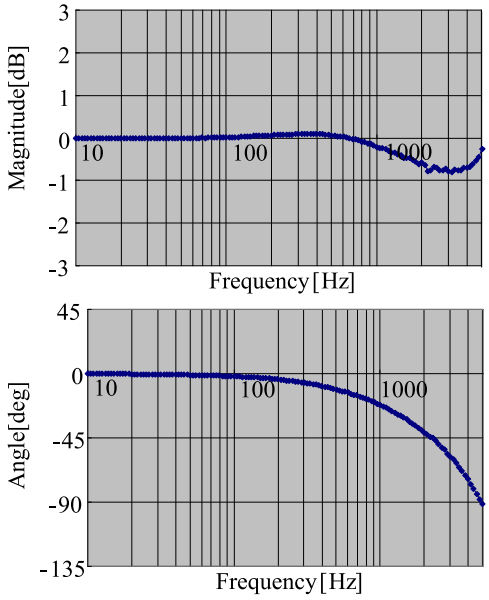


Figure 7 : Bode plot of the proposed current regulator (30[%] offset and 10[%] magnitude of rated current).

wave that has 30[%] offset and 10[%] amplitude of the rated current (Fig.6(a)) and step input (Fig.6(b)) of the rated value. In Fig.6(a), the red line is the analog q-axis current reference and the black line is the q-axis feedback current. In Fig.6(b), the violet line is the sampled current reference and the blue line is the sampled q-axis feedback current.

Fig.7 shows the Bode plot of the proposed current regulation using the FFT analyzer under the same condition as the Fig.6(a). At 2300[Hz], the magnitude is -0.77[dB] and the phase delay is -45[deg]. Hence, the bandwidth of proposed current regulator can be considered as 2300[Hz].

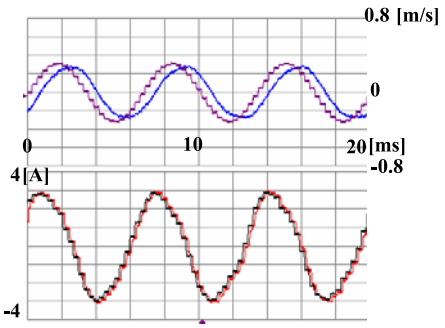


Figure 8 : Speed control performance of the proposed method (300[Hz] input).

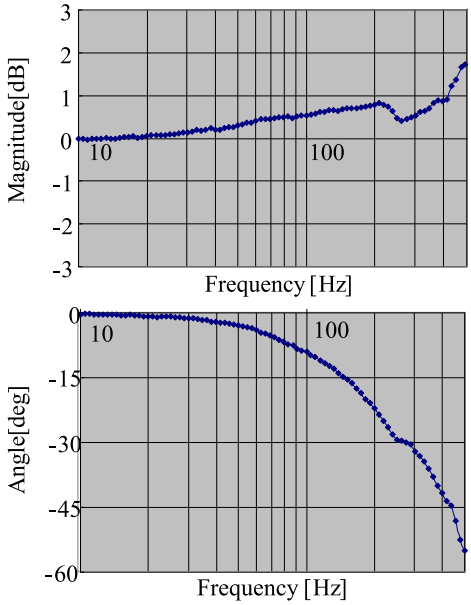


Figure 9 : Bode plot of the speed control with proposed current regulator.

Fig.8 demonstrates the performance of the speed control, when the speed reference is 300[Hz] sinusoidal wave that has magnitude of 0.03[m/s] at the peak. In Fig.8, the violet line is the speed reference, the blue line is the feedback speed, the black line is the q-axis current reference and the red line is the q-axis feedback current. As shown, the current regulation is performed well and the feedback speed tracks the speed reference under proposed speed control strategy.

In Fig.9, Bode plot of the speed control using the FFT analyzer is shown. At 440[Hz], the magnitude is 1.22[dB] and the phase difference is 45[deg], and the bandwidth of speed control can be considered as 440[Hz].

6. Conclusions

This paper proposes a novel design strategy of the current regulator which minimizes the digital delay, especially digital execution time and PWM delay. The bandwidth of the proposed current regulation can be extended up to 2.3[kHz] at 20 kHz sampling and 10KHz switching. And the extended bandwidth of the current regulator can improve the performance of the speed control of LSM. The experimental results reveal the performance of the proposed strategy. And the proposed current regulation and speed control strategies can be easily applied to any modern servo drive system run by the digital controller .

References

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